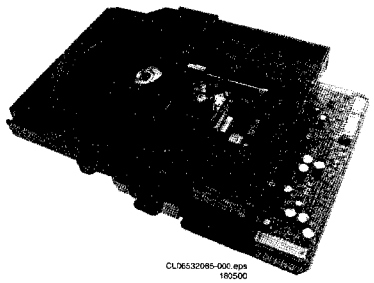
DVD-Video Player

DVD Module ASD-1

(Euro) 3104 129 21910
(Non euro) 3104 129 21920

Service
Service
Service



Service Manual

DVD VIDEO COMPACT disc DIGITAL VIDEO COMPACT disc DIGITAL AUDIO

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1. Technical Specifications

1.1 Connections

1.1.1 Connector 1600: Supply input connector.

1. +3V3stby
2. +3V3stby
3. +5V
4. +5Vstby
5. Vreserved
6. GND
7. GND
8. GND
9. -8Vstby
10. Standby control line
11. +12Vstby
12. GND

1.1.2 Connector 1603: A/V 1 connector.

1. P50
2. Blue Video
3. Green Video
4. GND
5. Red Video
6. CVBS
7. GND
8. Slow blanking scart
9. -8Vstby
10. +5V
11. +5V
12. Audio mute
13. GND
14. I2S data0 out
15. I2S wordselect
16. I2S bitclock
17. GND
18. I2S systemclock
19. Center_on
20. Kar_bypass
21. Kar_bypass
22. GND

1.1.3 Connector 1604: A/V 2 connector.

1. GND
2. Hor. sync.
3. GND
4. I2S data 2 out
5. GND
6. I2S data 1 out
7. -8Vstby
8. I2C clock
9. +12Vstby
10. I2C data
11. Vreserved
12. +3V3
13. GND
14. C video
15. GND
16. Y video

1.1.4 Connector 1501: I2C interface connector.

1. I2C clock
2. GND
3. I2C data
4. Standby control line
5. P50

1.1.5 Connector 1602: Service connector.

1. TXD
2. Service activation
3. RXD
4. Reserved for RTS
5. 5: GND
6. Reserved for CTS
7. +5V

1.2 Signal specifications

This the specification of all signals as described under "Connections"
H = +5V ±0.5V
h = 3V3 ±0.3V
L = 0V ±0.5V
l = 0V ±0.3V

Stby	:	If the set supports a "standby" function, all supply voltages marked with "stby" have to stay on during standby.
Standby control line	:	HStandby mode
	:	LOn mode.
P50	:	Connection between front and A/V board, and can be used as P50 signal line. The signal is not connected to the module electronics.
Slow blanking scart	:	This signal switches between
	:	0V (220Ωoutput impedance)
	:	12Vstby/2 (455Ω output impedance)
	:	12vstby (690Ω output impedance)
Audio mute	:	Can be used for audio mute transistors during stop or power on/off.
	:	Mute on : +5Vstby
	:	Mute off: -8Vstby via a 10kΩ resistor.
I2S data0 out	:	I2S front data output.
	:	Level h/l
I2S wordselect / I2S bitclock	:	I2S timing signals
	:	Level h/l
I2S systemclock	:	256xFS audio systemclock.
	:	Level H/L
Kar_bypass	:	Bypasses the karaoke chip on the A/V board.
	:	Bypass activeH
	:	Bypass offL
Center_on	:	Switches the center audio to the scart output.
	:	Center to scarth
	:	L/R to scartl
SPDIF out	:	Digital audio output
	:	Level H/L

Hor. Sync	:	Video Horizontal synchronisation
	:	Level h/l
I2S data1 out	:	I2S surround data output.
	:	Level: h/l.
I2S data2 out	:	I2S center/sub data output.
	:	Level h/l.
I2C clock / I2C data	:	I2C databus
	:	Level: H/L
TXD / RXD / RTS / CTS	:	Service UART to be connected direct to PC serial input.
	:	Output levelsH/L
	:	Input levelsRS232 compliant
Service activation	:	Signal openNormal module start-up
	:	Signal tied to GND Module start-up in service mode.
Vreserved	:	Reserved in case the A/V board requires an extra supply voltage.
	:	This supply is limited by a positive polarised 47uF/16V elco + 100nF/16V.

1.3 Performance:

1.3.1 Digital output

CDDA/LPCM	:	according IEC958
MPEG1 is converted to LPCM	:	
MPEG2, AC3 audio.	:	according IEC1937
DTS.	:	according IEC61937 amendment 1.
	:	Digital output level is 0V / 5V with GND as reference. To meet the standards a decouple circuit is necesary.

1.3.2 I2S output

Accuracy	:	Up to 24bit.
Sample rate	:	44.1kHz / 48kHz.
Standard	:	Philips I2S output
Number of I2S outputs	:	3 (6 channel: Front / Surround / Center-Bass)
Deemphasis	:	Already processed in module.
Audio source streams	:	CDDA / MPEG1 / LPCM / MPEG2 / AC3
	:	No DTS decoding.
Audio trick modes	:	Dolby Pro Logic (multichannel downmix on front output)
	:	3D sound.

1.3.3 Analog output

The module has no analog audio ouput.	:	The analog audio specification will be determined by the external DAC circuit.

1.3.4 Video.

Standards	:	The video output standard will follow the source material.
	:	The OSD standard is switchable between PAL or NTSC.
Outputs	:	The module has 6 analog outputs (3 formats): Y/C CVBS RGB.
Specification.	:	The output is fully according PQR3 IMS except
	:	Output load>1kΩ to GND / Cap. load <47pF.
	:	Level0.5Vpp with 100% white
	:	DC-levelSync bottom = -0.65V ±10%
	:	Some specification points are significantly better then PQR3
	:	SNR on all video outputs is better then 60dB.
	:	Video bandwidth >5MHz (±3dB)

2. Warnings and Laser safety instructions

(GB) **WARNING**

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).
Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential.

ESD

(NL) **WAARSCHUWING**

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).
Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.
Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.
Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

(F) **ATTENTION**

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).
Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise a leur manipulation.
Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.
Veiller a ce que les composants ainsi que les outils que l'on utilise soient également a ce potentiel.

(D) **WARNUNG**

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).
Unsorgfältige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern.
Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.
Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

(I) **AVVERTIMENTO**

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).
La loro longevita potrebbe essere fortemente ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione.
Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.
Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

(GB)

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

(NL)

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecifieerde worden toegepast.

(D)

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten.
Der Originalzustand des Gerats darf nicht verandert werden.
Fur Reparaturen sind Original-Ersatzteile zu verwenden.

(I)

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambiago idetici a quelli specificati.

(F)

Les normes de sécurité exigent que l'appareil soit remis a l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.

SHOCK, FIRE HAZARD SERVICE TEST:

CAUTION: After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,
Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer.
Ref.UL Standard NO.1492.

NOTE ON SAFETY:

Symbol ⚠ : Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol ⚠
Any other component substitution(other than original type), may increase risk or fire or electrical shock hazard.

"Pour votre sécurité, ces documents doivent être utilisés par des spécialistes agrées, seuls habilités à réparer votre appareil en panne."

LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

LASER DEVICE UNIT

Type:	SemiconductorlaserGaAlAs
Wave length:	650 nm (DVD)
	780 nm (VCD/CD)
Output Power:	7 mW (DVD)
	10 mW (VCD/CD)
Beam divergence:	60 degree

USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

AVOID DIRECT EXPOSURE TO BEAM

WARNING

The use of optical instruments with this product will increase eye hazard.
Repair handling should take place as much as possible with a disc loaded inside the player

WARNING LOCATION: INSIDE ON LASER COVERSHIELD

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

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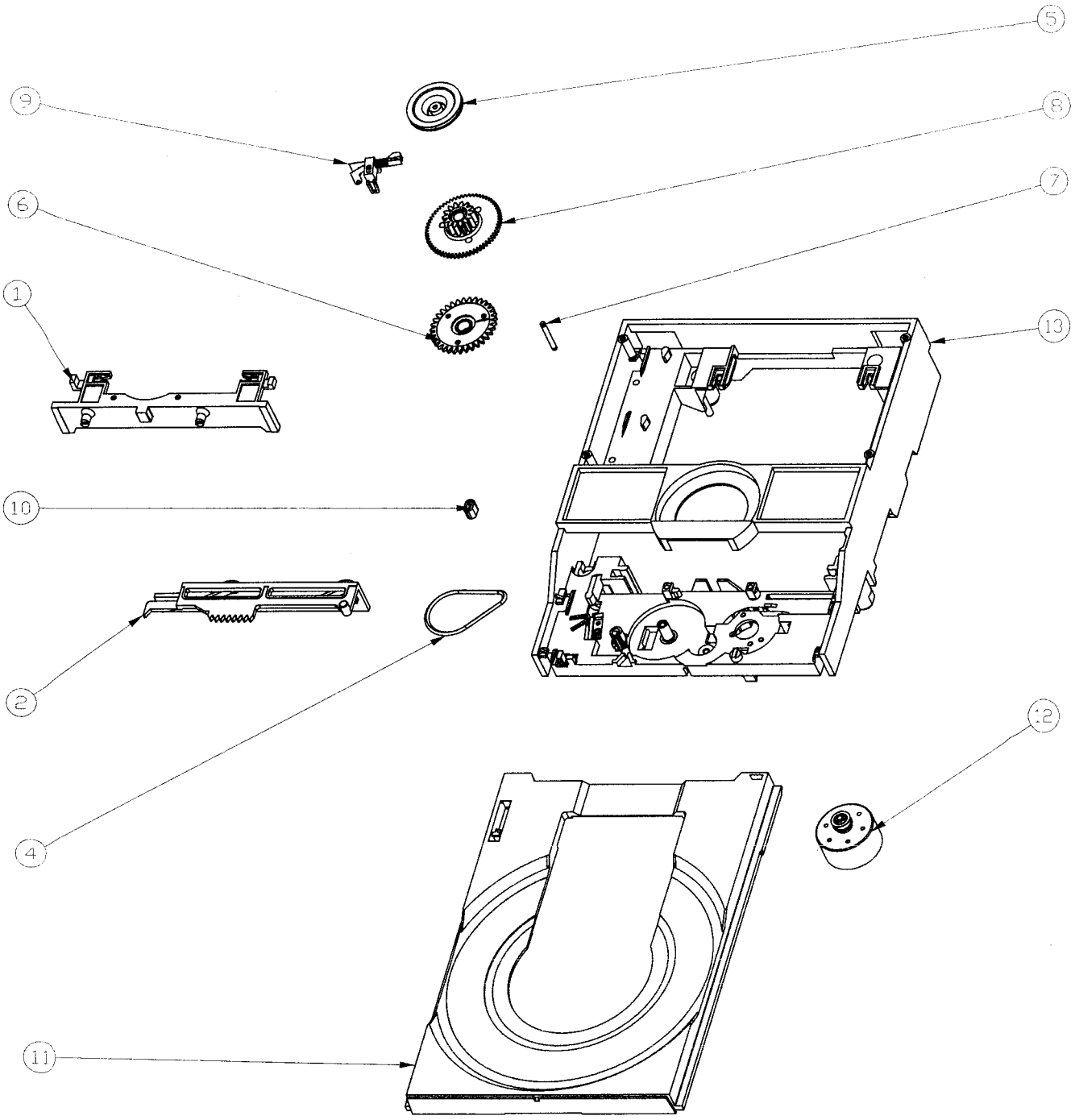
230500

3. Directions for use

There is no DFU available

4. Mechanical instructions



4	4822 358 10266	BELT
9	3139 198 80010	SWITCH
10	4822 532 13097	TULE
11	3139194 00270	TRAY
12	3139 197 50060	TRAY MOTOR ASSY

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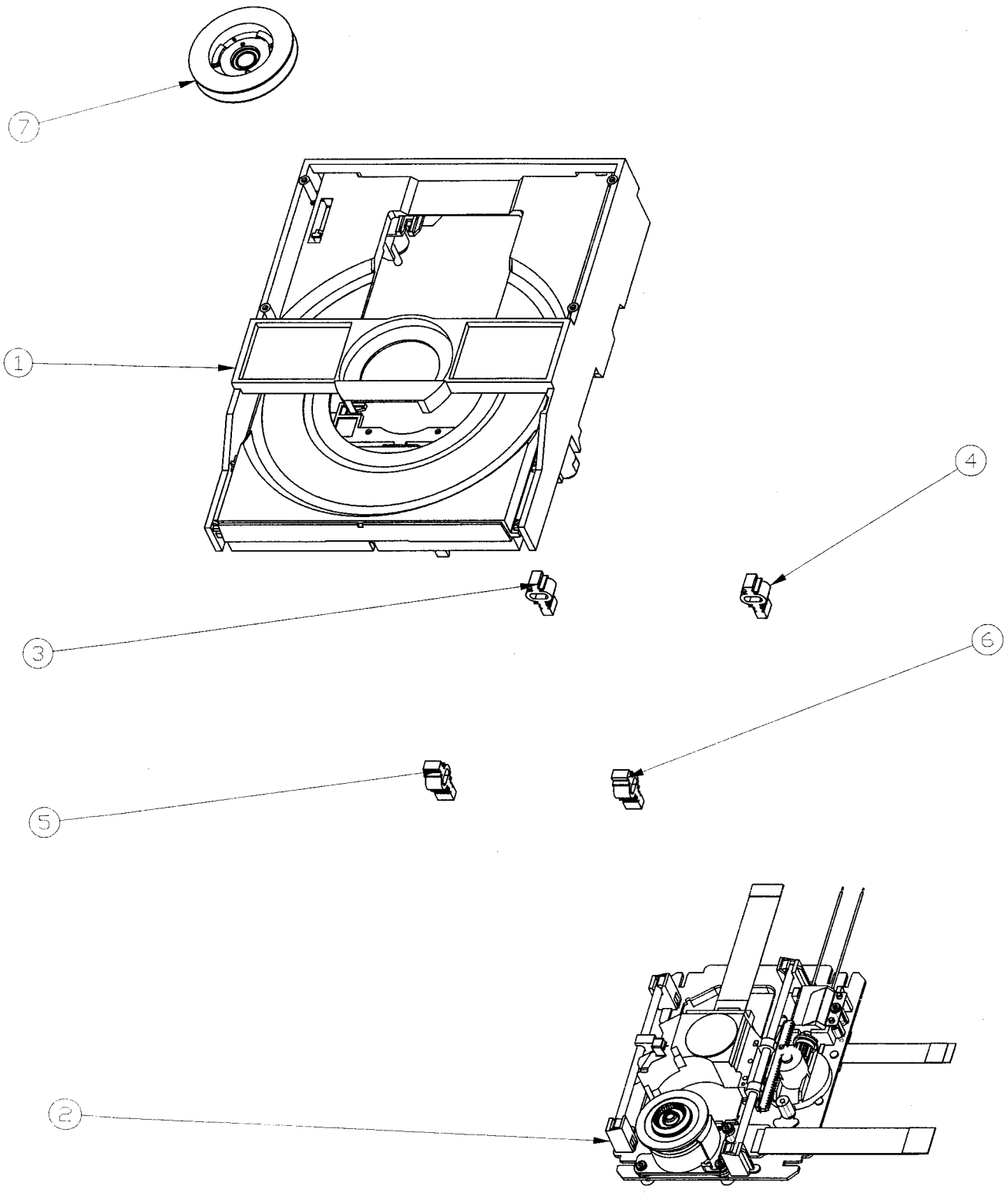
180500



	9305 023 61101	VAL6011/01 LOADER COMPLETE
1	3139 197 60090	GENEVA LP LOADER ASSY
2	9305 022 60101	VAM6001/01
3+4	3139 194 00710	SUSPENSION (YELLOW)
5+6	3139 194 00620	SUSPENSION (BLUE)
7	3139 197 60060	CLAMPER ASSY

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180500

5. Test instructions mono board DVD-ASD1

5.1 General

- Impedance of measuring-equipment should be > 1MΩ.
- Most tests have to be done by software commands. Together with the software command you will find a Ref.# nbr. This is the number of the diagnostic nulceus used for this test. More detailed information can be find in the chapter "Diagnostic Nuclei".
- Levels: Most measurements are digital measurements. The high and low levels in this document got to have next specification:
  low : < 0.3V
  high : > 3.0V
  LOW : < 0.4V
  HIGH : > 4.5V
- All voltages marked with "stby" have to stay on during standby.

5.2 General start-up measurements

5.2.1 Supply check:

Pin nbr.	Supply
1600-1	3V3
1600-2	3V3
1600-3	+5V0V during STAND BY
1600-4	+5Vstby
1600-5	+6V
1600-6	0V
1600-7	0V
1600-8	0V
1600-9	-8V
1600-10	0V5V during STAND BY
1600-11	+12Vstby

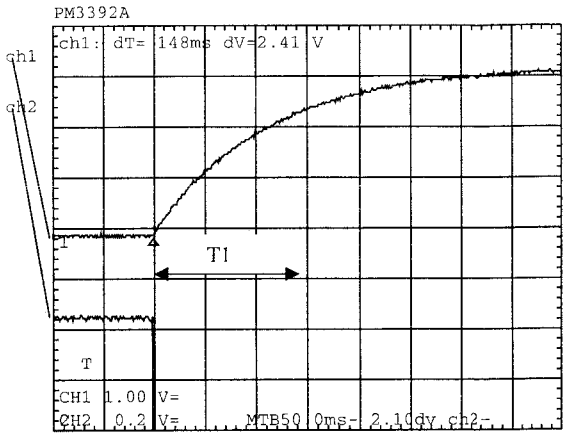
0V

Check the supply currents to be sure there are no large failures on the board. Before measuring the currents, make sure that no A/V board, display board or Mercury 1 loader is connected to the mono board and that the PC interface cable is connected to the board.
Also check if the servo part gets its power.
Testpoint F608: +3V3 ±5%
Testpoint F101: +9V ±5%
The supply currents can be measured using a Tektronix AM503B current probe.

Supply	power consumption	
3V3	400mA ±10%	
5V	370mA ±10%	
5Vstby	< 5mA	
-8V	55mA ±10%	fluctuation: ±20mA
12Vstby	30mA ±20%	fluctuation: ±150mA

5.2.2 Reset check:

The reset circuit is triggered by the stand-by line. First make sure that the STB_CONT line is HIGH by connecting 5V to testpoint F505.
Then switch STB_CONT over to LOW and check next timing at the STI5505 reset input (testpoint F503):



RESET TIMING CL06532065_003.eps 180500

Figure 5-1

T 1 = 150msec ±25% (From 0V to 3V3 -3db)
If the reset input doesn't go high then check the circuit around transistor 7501.

5.2.3 Clock check

To check the correct functioning of the STI5505, we first have to check the presence of all clocks.
All clocks to be measured with 0.02% tolerance.

Clock-name	Testpoint	Frequency
27M_CLK	F051	27MHz
PCM_CLK	F566	11.2896MHz

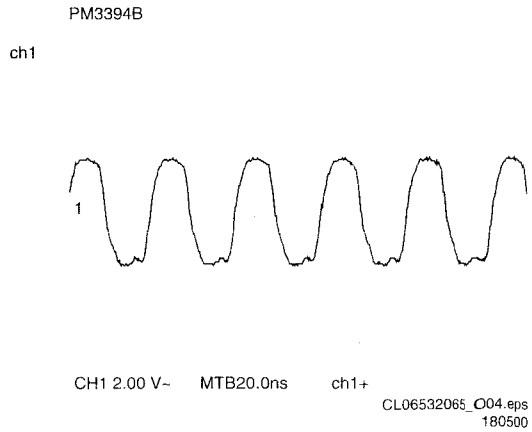


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Figure 5-2

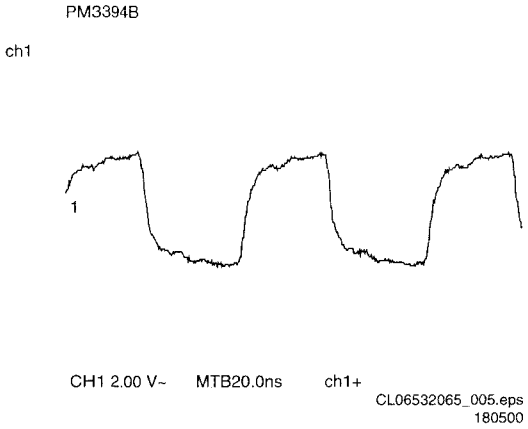


Figure 5-3

5.3 µP environment:

5.3.1 General:

All the tests are carried out by software tests. To start the software tests, connect a PC to the serial bus of the STI5505. Use connector 1602 for this connection:

Connector pin	Signal
1602-1	TXD (STI5505 out)
1602-2	Service-mode select
1602-3	RXD (STI5505 in)
1602-4	RTS (STI5505 out)
1602-5	GND
1602-6	CTS (STI5505 in)
1602-7	+5V

Now start the terminal program. Make sure that the service-pin of the µP is pulled low (pin 1602-2) and then reset the µP (make the STB_CONT line low). The terminal program of your PC should now display: "DVD2 Diagnostic software version ...". This message already means that the µP is running. The first 5 commands from the diagnostic software will be carried out automaticly during diagnostic start-up. The other commands can be carried out by selecting the "command input". Just type the reference nbr. to do the test.
To be sure that the µP is able to run the diagnostic software, serial port will be checked during start-up.

Ref. #	Reference Name	Remark
(1)	BasicSpAcc	Serial port Access test/initialisation
(2)	BasicDramWrR	DRAM Write Read

5.3.2 Memory check:

The µP has a data bus that is connected to a DRAM (not present!!) and a Flash.
The µP has also an internal link to the MPEG SDRAM interface.
Next databus checks will be done at start-up to check this data-bus and SDRAM bus.

Ref. #	Command Name	Remark
(2b)	BasicInterconSDRAM	Data and address bus Interconnection
(2c)	BasicInterconFlash	Data and address bus Interconnection

There are 2 memory checks left that can be done by hand command

Ref. #	Command Name	Remark
6	PapChksFl	Checksum FLASH
16	CompSdramWrR	SDRAM Write Read

5.4 General I/O port & peripherals check

5.4.1 I2C bus / EEprom check

To access the EEprom, the I2C bus is used. So by writing and reading to the EEprom the chip and the bus is checked. With next commands a certain byte is written to the EEprom. The original information will always be written back into the EEprom.

Ref. #	Command Name	Remark
11	PapI2cNvram	I2C NVRAM access

The complete Eeprom can also be checked on failures by writing to all addresses and reading back. This test takes a long time (110 sec).

Ref. #	Command Name	Remark
15	PapNvramWrR	NVRAM Write Read

5.4.2 Audio clock switch check

For a DVD disc the audio clock has to be switched from 44.1KHz sampling to 48KHz sampling.
To do so IO-port 1 / 4 has to be switched. Send next commands and check the audio-clock

Ref. #	Remark	Testpoint	Frequency
7a	(Clock A_CLK in 44.1kHz mode)	F566	11.2896MHz ± 0.02%
7b	(Clock A_CLK in 48kHz mode)	F566	12.288MHz ± 0.02%

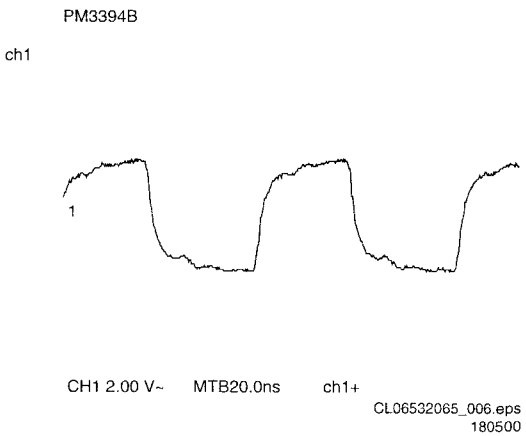


Figure 5-4

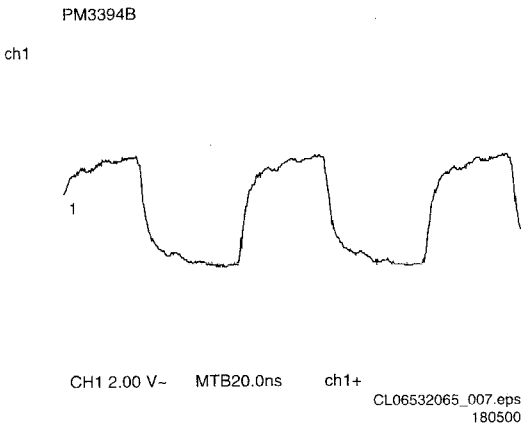


Figure 5-5

5.4.3 Audio deemphasise check

The STI5505 output pins PIO 4-0 and PIO 4-1 were used to switch deemphasis on a previous type of DAC. This function is not used anymore, because deemphasis is done internally in STI5505, but the name still remains. The lines are now used for a series of functions such as centre_on_stereo or karaoke_bypass. The PIO 4-0 has got a pull-up to +5V and the PIO 4-1 has not. To check these pins these commands can be used.

Ref. #	Command Name	Remark Testpoint	Value
18e	AudioDeemp0TristateOn	PIO 4-0 Tristate On	------
56a	AudioDeemp0On	PIO 4-0 OnF630	HIGH
56b	AudioDeemp0Off	PIO 4-0 0 OffF630	low
18f	AudioDeemp0TristateOff	PIO 4-0 Tristate Off	------
56c	AudioDeemp1On	PIO 4-1 OnF633	high
56d	AudioDeemp1Off	PIO 4-1 OffF633	low

5.4.4 Audio mute check

Switch on the Mute circuit by sending next command:

Ref. #	Command Name	Remark
19a	AudioMuteOn	AudioMuteOn

Check the Mute output again at testpoint F625: 4.7V ±10%
Switch off the Mute circuit by sending next command

Ref. #	Command Name	Remark
19a	AudioMuteOff	AudioMuteOff

Check the Mute output at testpoint F625: -8V ±10%

5.4.5 Audio I2S check

To check the audio output, connect a audio DAC to the I2S output (DVD950 A/V board) and start-up the audio test. Look at the audio outputs from the A/V board for both sine and pink noise.

Ref. #	Command Name	Remark	Audio outputs
21a	AudioSineOn	Audio Sine signal Off	Audio Sine signal On Sine, 1kHz on stereo Press stop button
20a	AudioPinkNoiseOn	Audio Pinknoise On	Pink Noise on 6 channels
20b	AudioPinkNoiseOff	Audio Pinknoise Off	

The audio signal (sine or pink noise) will also be present on the digital ouput (SPDif). This can be checked by connecting an amplifier with digital input.
Check the I2S output.
LRCLK at testpoint F641

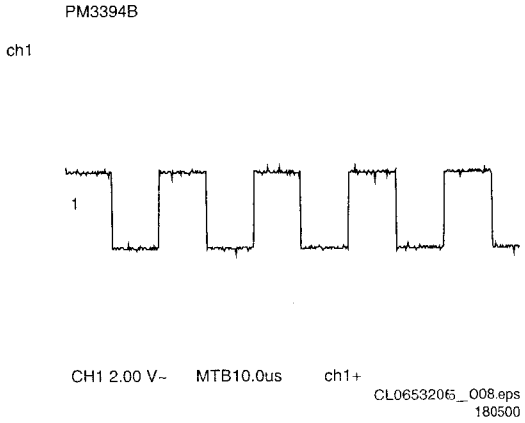


Figure 5-6

SCLK at testpoint F637

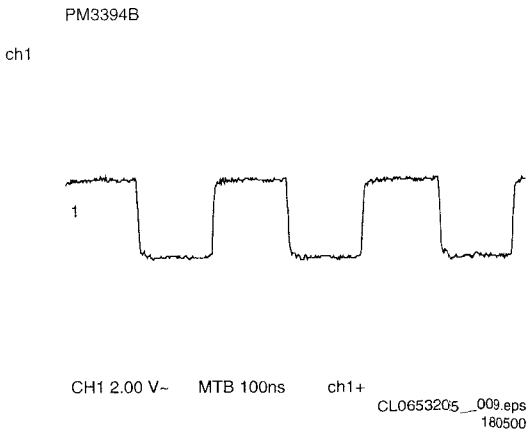


Figure 5-7

PCM_OUT0 at testpoint F638
PCM_OUT1 at testpoint F659
PCM_OUT2 at testpoint F658

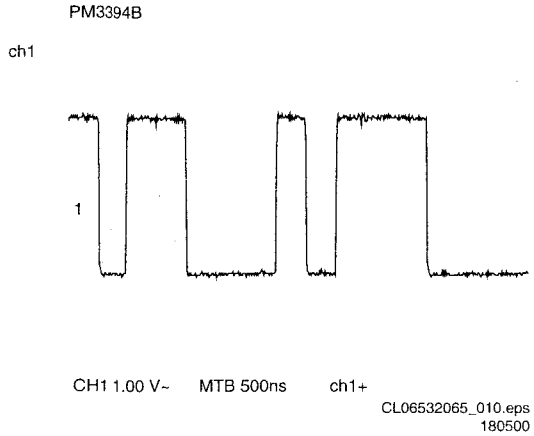


Figure 5-8

PCM_CLK at testpoint F640

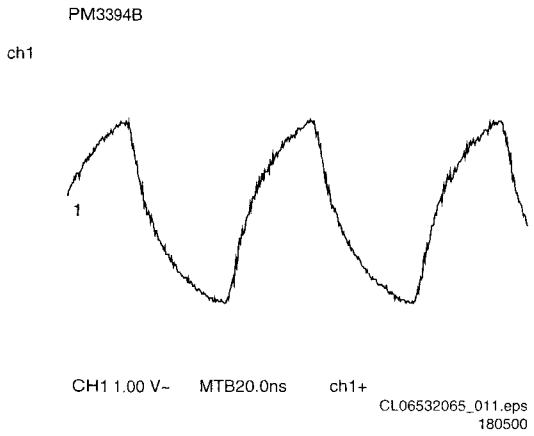


Figure 5-9

SPDIF at testpoint F644

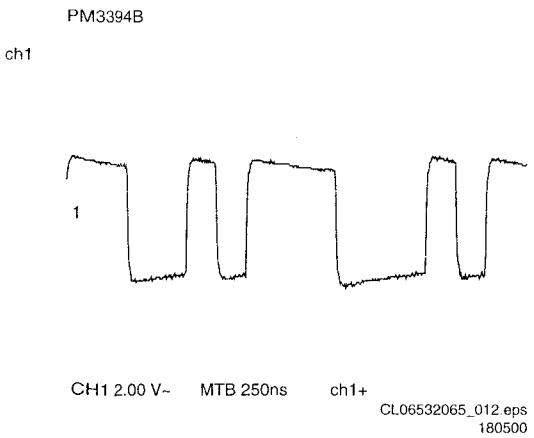


Figure 5-10

To switch the audio signal off, press the STOP button on the front.
Without A/V board all levels should be switching between low and high except:

- PCM_OUT1 and PCM_OUT2 only between low and high for pink noise. For sine, this is low.
- PCM_CLK and SPDIF switches between LOW and HIGH

Alternatively, there is a check that can be done without A/V board.
First, let the decoder generate pink noise on the audio outputs.

Ref. #	Command Name	Remark
20a	AudioPinkNoiseOn	Audio Pinknoise On

Measure then these signals on level and frequency.

Signal	Level between	Frequency
LRCLK	low/high	48kHz ± 0.02%
SCLK	low/high	3.072MHz ± 0.02%
PCM_CLK	LOW/HIGH	12.288 MHz ± 0.02%
PCM_OUT0, 1, 2	low/high	N/A
SPDIF	LOW/HIGH	N/A

Put the pink noise off:

Ref. #	Command Name	Remark
20b	AudioPinkNoiseOff	Audio Pinknoise Off

5.5 VIDEO

5.5.1 Video output check

Check DC output-level at all video-outputs at conn 1603-2,3,5,6 and conn 1604-16: -0.65V ± 10%
Generate a color-bar via next software commands:

Ref. #	Command Name	Remark
23a	VideoColDencOn	Colourbar DENC On
23b	VideoColDencOff	Colourbar DENC Off

Check video output at the next testpoints:
F646: R_VID

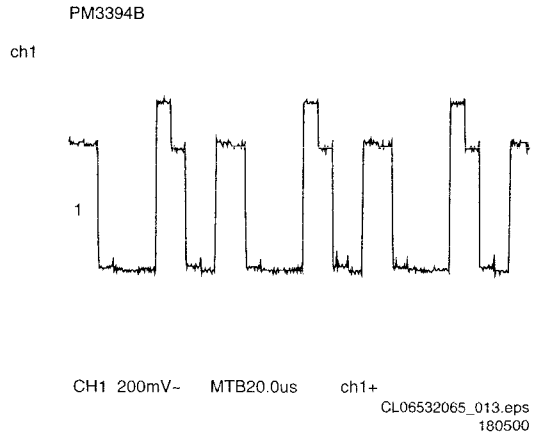


Figure 5-11

F649: G_VID

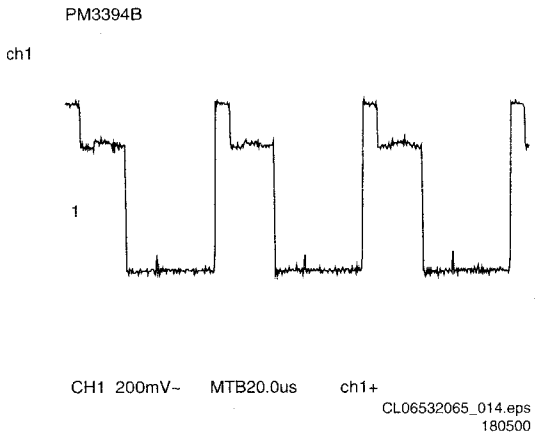


Figure 5-12

F653: B_VID

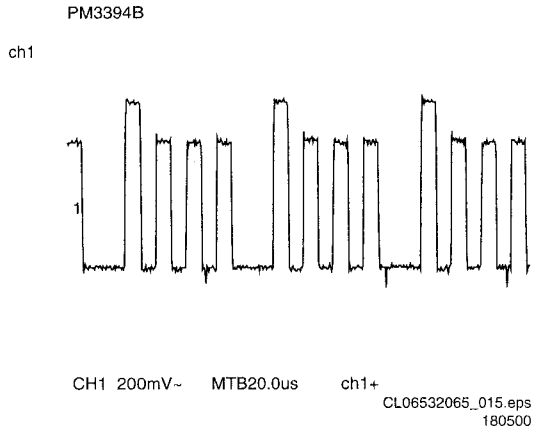


Figure 5-13

F657: CVBS

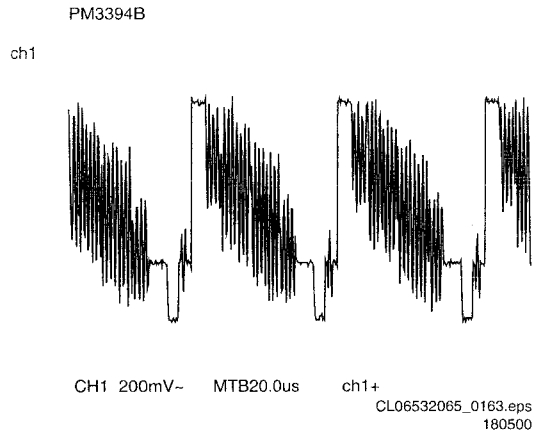


Figure 5-14

F665: C_VID

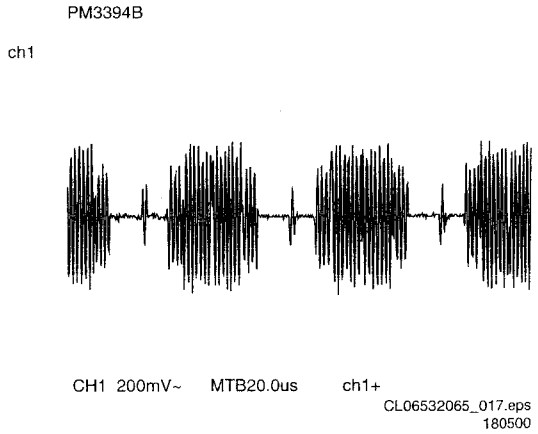


Figure 5-15

F666: Y_VID

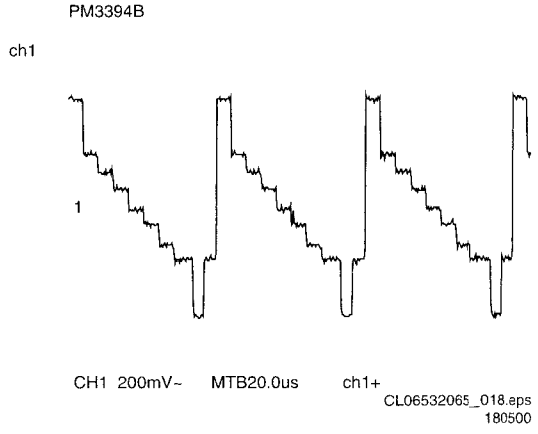


Figure 5-16

5.5.2 Scart-switching voltage

An aditional part of the video-path is the scart-switching voltage.
This voltage can be 0V, 6V, 12V.
Check at testpoint F620 the output-voltage while using next commands:

Ref. #	Command Name	Remark
25a	VideoScartLo	Sends out 0V ± 0.5V
25b	VideoScartMi	Sends out 6V ± 10%
25c	VideoScartHi	Sends out 12V ± 10%

5.5.3 Video Hsync check.

To measure the correctness of this output, F656 should be checked.

Ref. #	Command Name	Remark	Value
23a	VideoColDencOn	Colourbar	DENC on15.625 kHz ± 0.02% Vpeak-peak > 3V
23b	VideoColDencOff	Colourbar	DENC off No measurements needed

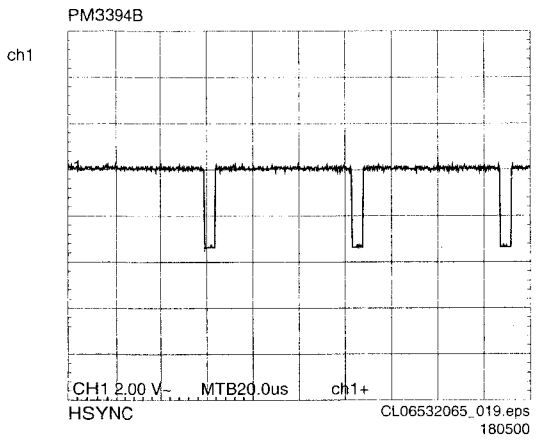


Figure 5-17

5.6 Servo

5.6.1 General start-up measurements:

Reset the Basic Engine part

Ref. #	Command Name	Remark
44	BeReset	Basic Engin

Check Vref

Name	Testpoint	Value
Vref	F188	2.5V+/-0.3

Check I2S interface

Name	Testpoint	Value
B_BCLK	F347	6.0MHz +/-0.1

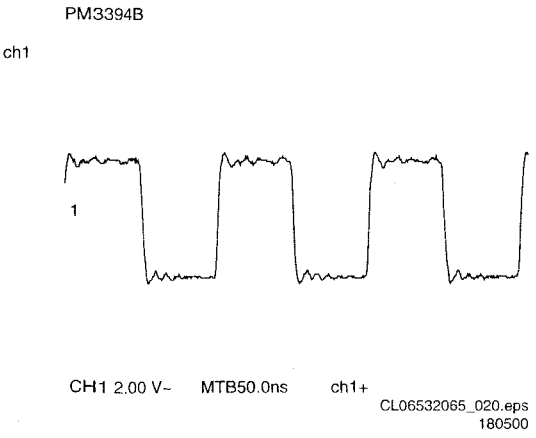


Figure 5-18

CL1F33712.0MHz +/-0.2

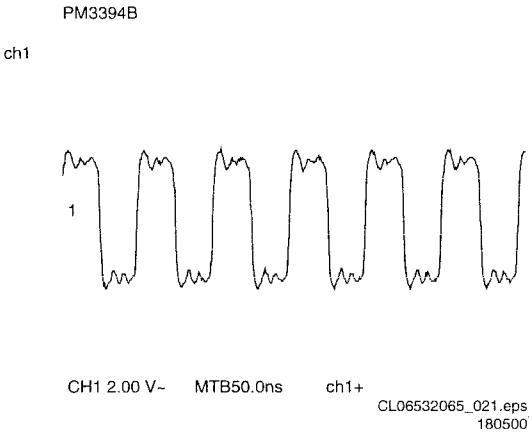


Figure 5-19

B_WCLKF343HIGH
StopclkF338HIGH
B_SyncF344HIGH
B_V4F348HIGH

5.6.2 Spindle Motor:

Before switching on the discmotor, check the following testpoints:

Name	Testpoint	Value
Stby	F357	high
Stby-out	F355	LOW
Moto1	F361	3V±0.3

Switch the Discmotor on/off with next commands:

Ref. #	Command Name	Remark
39a	BeDiscmotorOn	Discmotor on
39b	BeDiscmotorOff	Discmotor off

Check the following signals when discmotor has been switched on::

Name	Pin nr.	Frequency
Stby	F357	low
Stby-out	F355	HIGH
Moto1	F361	3V±0.5V
A3	F350	see oscillogram
A2	F352	see oscillogram
A1	F353	see oscillogram

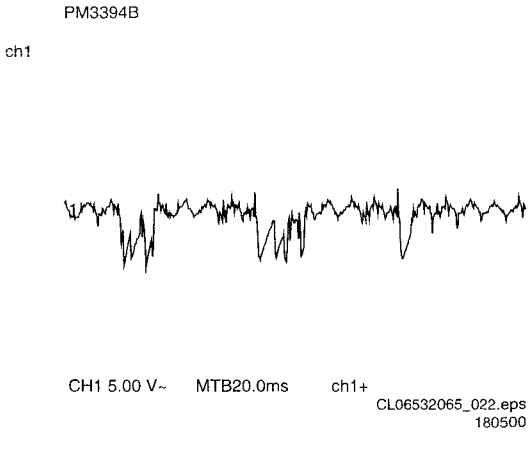


Figure 5-20

T1	F280	see oscillogram
T2	F368	see oscillogram
T3	F371	see oscillogram

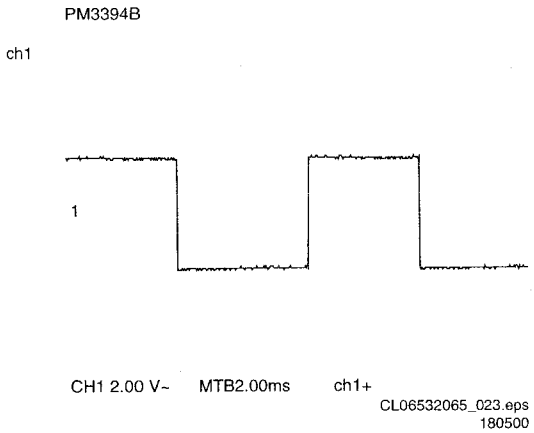


Figure 5-21

VH	F365	3V±0.5V
H1+	F354	see oscillogram
H1-	F359	see oscillogram
H2+	F364	see oscillogram
H2-	F366	see oscillogram
H3+	F367	see oscillogram
H3-	F370	see oscillogram

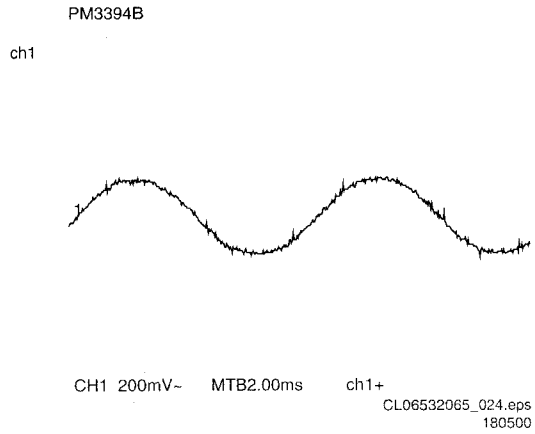


Figure 5-22

Switch the discmotor off.

5.6.3 Radial

Swith the radial control on/off with the following commands:

Ref. #	Command Name	Remark
40a	BeRadialOn	Radial control on
40b	BeRadialOff	Radial control off

Check the following signals:

Name	Testpoint	Value
Rad -	F128	4.3V±0.5V
Rad +	F121	4.3V±0.5V

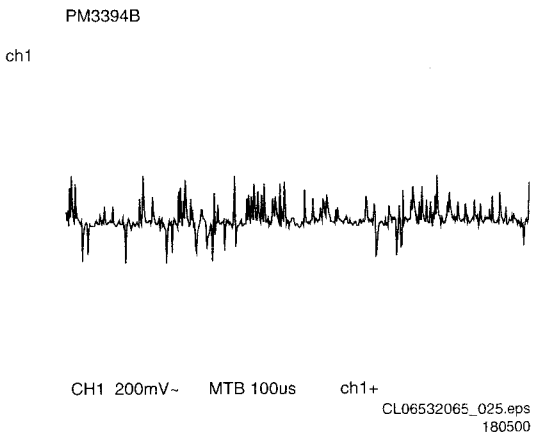


Figure 5-23

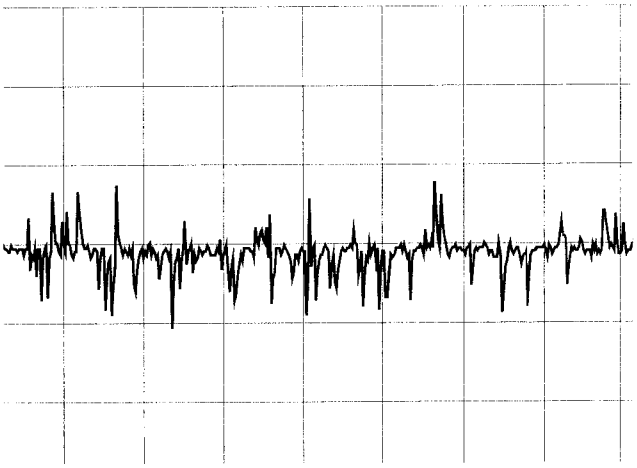


Figure 5-24

Check for pulse density signal RA at testpoint F227

Figure 5-25

Check if laser is switched on (visual check of laser light).
Switch the radial control off.

5.6.4 Sledge

Use the following commands to move the sledge:

Ref. #	Command Name	Remark
41a	BeSledgeIn	Sledge inwards
41b	BeSledgeOut	Sledge outwards

Check pulse density signal SL at testpoint F221

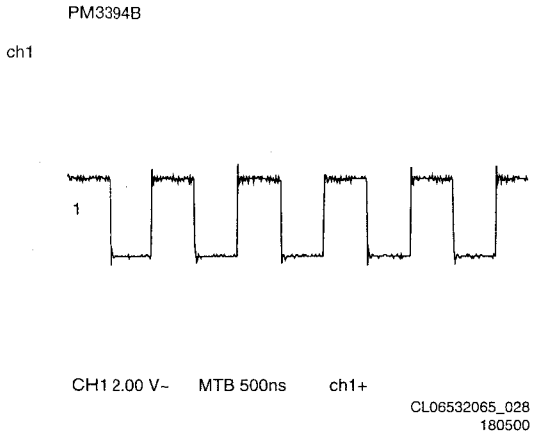


Figure 5-26

Name	Testpoint	Value
SI -	F012	4.5V±0.5V
SI +	F011	4.5V±0.5V

Measure peak to peak signal on SL- and SL+ while moving sledge outwards.

Name	Testpoint	Value
SI -	F012	10Vptp +/-0.5
SI +	F011	10Vptp +/-0.5

Measure input sledge control (sledge in home position)

Name	Testpoint	Value
Sinph	F182	2.2V±0.5V
Cosph	F192	2.2V±0.5V

5.6.5 Tray:

To open and close the tray use the following commands:

Ref. #	Command Name	Remark
43a	BeTrayIn	Tray in
43b	BeTrayOut	Tray out

Measure the driver outputs of the BA5938FM for the tray closed.

Name	Testpoint	Value
Vo2 -	F116	4.3V±2.0V
Vo2 +	F111	4.3V±2.0V

Measure again the driver outputs while the tray is opening.

Name	Testpoint	Value
Vo2 -	F116	2.0V±1.0V
Vo2 +	F111	6.0V±1.0V

5.6.6 Focus

To switch the Focus motor on/off, use the following commands:

Ref. #	Command Name	Remark
38a	BeFocusOn	Focus on
38b	BefocusOff	Focus off

Measure the driver outputs of the BA5938FM for the Focus off.

Name	Testpoint	Value
foc -	F124	4.3V±0.5V
foc +	F127	4.3V±0.5V

Switch the focus on

Measure again the driver outputs

Name	Testpoint	Value
Foc - (sawtooth)	F124	1V±0.2V
Foc + (sawtooth)	F127	1V±0.2V

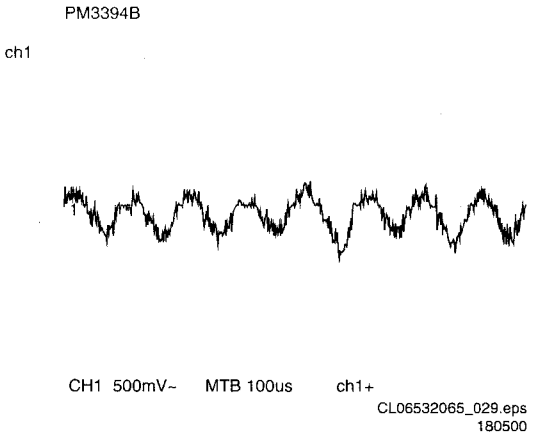


Figure 5-27

Check for pulse density signal FO at testpoint F234

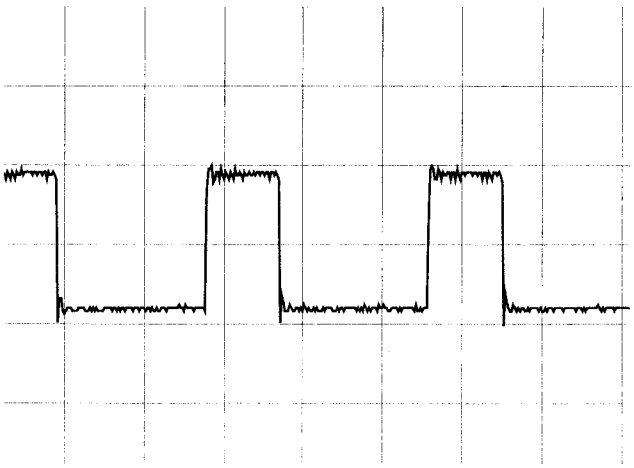


Figure 5-28

Check for laserlight.

Switch the focus off

5.6.7 Hf path

Play DVD test disc.

Measure outputs of diodes A, B, C, D, E, F.

Name	Testpoint	Value
A	F140	2.6V±0.2V
B	F141	2.6V±0.2V
C	F143	2.6V±0.2V
D	F144	2.6V±0.2V
E	F147	2.6V±0.2V
F	F148	2.6V±0.2V

At outputs of diodes A, B, C, D the following oscillogram can be measured:

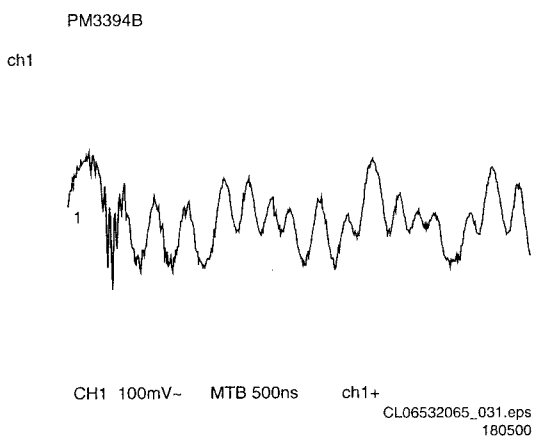


Figure 5-29 cl06532065-031

Measure DVDALAS outputs

Name	Testpoint	Value
RFO DC	F146	2.5V ±0.2V
O1	F156	25mV±10mV
O2	F159	25mV±10mV
O3	F169	25mV±10mV
O4	F166	25mV±10mV
S1	F174	25mV±10mV
S2	F175	25mV±10Mv

At output RFO, the following oscillogram can be measured:

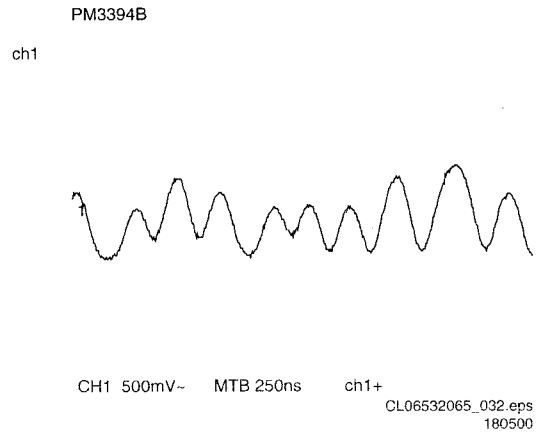


Figure 5-30

5.7 Diagnostic software description Introduction

5.7.1 Introduction

Purpose

This document describes all interfaces from the outside world to the diagnostic software, what is needed to use these interfaces and how to access them.
Changes for DVDv2b are marked.

Scope

This document has been realised within the framework of the product development of the second generation DVD video player. This player forms the basis for future DVD developments as described in the DVDv2 Overall Project Management Plan.

5.7.2 Definitions and abbreviations

Definitions

Control PC	Automatic test equipment, part of the production control system in the factory, to control the execution of Diagnostic Nuclei in the DVD player.
Diagnostic Nucleus	Part of the Diagnostic Software. Each nucleus contains an atomic and software independent diagnostic test, testing a functional part of the DVD player hardware on component level.
Script	Part of the Diagnostic Software. Each script contains a sequence of Diagnostic Nuclei to be executed.
Service PC	PC used by a service- or repair-person to communicate with the Diagnostic Software in the DVD player.

Abbreviations

FDS	Full Diagnostic Software

5.8 Overview of Interfaces

The table below shows an overview of the user interfaces of the Diagnostic Software. The table is based on logical interface, interfaces as seen from user perspective. A logical interface can use one or more physical interface components. The DVD has only a single RS232 port, implying that all interfaces using this port are mutually exclusive.

Logical Interface	Description	Physical interface components
Menu Interface	Menu-driven activation of individual nuclei, used for Level 2/ Second Line diagnostic mode. Users are service or repair people	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin
Command Line Interface	Used during Level 1 diagnostic mode. Used to send commands from the Control PC into the DVD hardware.	Control PC, running a control program (e.g. Asterix), connected to RS232 port of the DVD player Test pin
Script Interface	Used to execute Player Test Script (including reading the error log) and Dealer Test Script.	Local keyboard Local display
S2B interface	Used for S2B communication with the Basic Engine	Service PC, running a S2B monitor program, connected to the RS232 port of DVD player Test pin
Download Interface	Used to download diagnostic software into the DVD player	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin

In the next chapters the logical user interfaces are described in more detail including the exact use of the physical interface components.

5.9 Description Of Interfaces

5.9.1 Menu Interface

The menu interface is part of the Level 2 / Second Line diagnostic mode. Via the menu interface it is possible to control the execution of the Diagnostic Nuclei.

Set-up physical interface components
Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

5.9.2 Code nr. PC interface cable: 3122 785 90017

Activation
Switch the player on and the following text will appear on the screen of the terminal (program):

```
DVDv2 Diagnostic Software version 1.0


SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK


(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@M <-
<main menu>
Select>
```

CL06532065-033.eps
180500

The first line indicates that the Diagnostic software has been activated and contains the version number of the diagnostic; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully. The next three lines are the succesful result of the subsequent basic tests (nuclei 2, 3, 4 and initialisation of Karaoke chip respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The last line is the prompt asking to choose for an interface form. If a choice for Menu Interface has been made, the main menu will appear. For the layout of the menus, see page 25.
To switch between interfaces, the DVD player needs to be switched off and on again.
Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.
Note2 : The Dram tests are no longer executed because the player has no DRAM .
Note3 : When the stack is located in the internal memory, the test with the SRAM doesn't work and will be left out.
Note4 : The karaoke initialisation will also take place if there is no karaoke-chip in the player.

Usage
A selection can be given by the user by typing the number of the menu-item chosen at the prompt. Each entry must be terminated with a . Invalid selections will cause an error message by the Menu Handler. Example:

```
Select > 60
0001 Invalid menu selection ER @
Press RETURN to continue...@
```

CL96532111_021.eps
071099

Result and output of an activated (and terminated) nucleus will be sent back to the service terminal. Example:

```
Select > 16
1601 Data line X is not connected to the SDRAM ER @
Press RETURN to continue...@
```

CL96532111_022.eps
071099

After the user presses a key, the current menu is rebuilt on screen.
Pressing < return > at the prompt without any further input at the terminal will always rebuild the main menu.

Termination
The menu interface is terminated by switching off the DVD player.

5.9.3 Command Line Interface

The command line interface is part of level 1 diagnostic mode. Via a command line interface the execution of Diagnostic Nuclei can be controlled.

Set-up physical interface components
Hardware required:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to the Control PC

The control PC must use the following port settings for the used COM port: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The control PC is connected with a special cable to the RS232 port of the DVD player. Via the same connection the test pin will be connected to ground.

Activation
After power on the next text will sent to the control PC

```
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@ C <-
DD>
```
CL06532065_034.eps
180500

The first line indicates that the Diagnostic software has been activated and contains the version number; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully. The next three lines are the succesful result of two subsequent basic tests (nuclei 2, 3, 4and karaoke initialisation respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The fifth line lets the user choose between the two possible interface forms. The last line is the prompt ("DD>"). The diagnostic software is now ready to receive commands.
Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.
Note2 : When it is a player without DRAM, the DRAM tests are left out.

Usage
The commands that can be given are the names or the numbers of the nuclei. A command must be terminated with a < return > character from the control PC. When typing commands, the backspace key can be used to make corrections.
In case of typing errors in the command, an error message is returned. Example:

```
DD >CompSdarmWrR
0001 Unknown command ER @
DD>
```
CL96532111_024.eps
071099

If the command (the nucleus name or number) is recognised, the nucleus is executed. Result and output of an activated (and terminated) nucleus will be sent back to the control PC according to the standard layout as defined in Appendix C.

Example in case the command is correct:

```
DD >CompSdarmWrR
1600 OK @
DD>
```
CL96532111_025.eps
071099

Example in case the result is an error:

```
DD >CompSdarmWrR
1601 Address line X not connected to the SDRAM @
DD>
```
CL96532111_026.eps
071099

Termination
The command line interface is terminated by switching off the DVD player.

5.9.4 S2B Interface (not for service)

Set-up physical interface components
Hardware needed:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to Control PC
- S2B monitor tool running on the Control PC

Activation
To start the S2B interface, connect the RS232 cable to the Control PC in the correct manner. Then start the PC, start the monitor tool and start the DVD player; turn off the monitor tool, turn on S2B monitor tool. The S2B monitor tool now takes all communication.
The S2B interface is activated by sending the bit pattern 110x xxxx with the first character to the DVD player, when the user is asked to choose an interface type. The command handler will then activate the S2B pass-through nucleus. The character sent will be passed to this nucleus without loss.
Note: The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

Termination
To terminate S2B pass-through mode, switch off the DVD player.

5.10 Script Interfaces

This interface is used during execution of the Player Script and the Dealer Script to display output and error messages.
The local display will be used to display the output and the error messages.

5.10.1 Dealer Script

Set-up physical interface components
Hardware required:
- DVD player

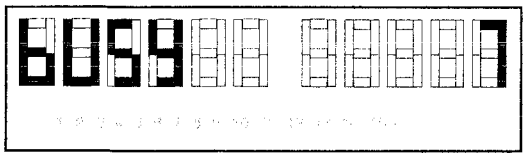
The DVD player is tested stand-alone: no other equipment than the DVD player is needed.

Activation
The dealer script is activated by pressing OPEN/CLOSE and PAUSE on the local keyboard of the DVD player simultaneously during power-on.

Note : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

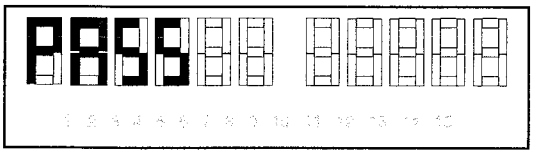
Usage

The test requires no user interaction. A number of nuclei will be run before a message is returned indicating if there is a failure in the DVD player.
During the execution of a script, a progress indicator is displayed on the local display of the DVD player.

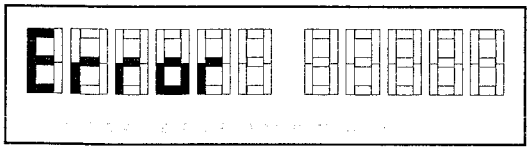


CL96532111_017.eps
071099

The counter at the right side of the display counts down from the number of nuclei to be run to zero. At zero all nuclei from the script have been run and the result (PASS/Error) is displayed on the local display of the DVD player.
When the dealer script has been completed, the results are displayed in the following manner:



CL96532111_018.eps
071099



CL96532111_019.eps
071099

Termination

To turn off the dealer test, the DVD player must be powered down.

5.10.2 Player Script

Set-up physical interface components

Hardware needed:

- DVD player
- television set, connected to the DVD player
- 6 audio speakers
- an external video source

Activation

To activate the player script, press OPEN, CLOSE and STOP keys on the local keyboard of the DVD player simultaneously during power-on.

Usage

The player test requires human interaction to decide whether nuclei give correct output, e.g. the user needs to confirm the results of the display test. This needs to be given through the local keyboard on the DVD player. Which keys can be used for this purpose is described with each test.
Module test (with user interaction)
During the first phase of the dealer test, the three main modules (Digital PWB, Display PWB and Basic Engine) are tested; some interaction from the user is required.
1. Testing the Display PWB
This involves testing the local display and keyboard, but also testing the remote control and the leds.

The Display Test

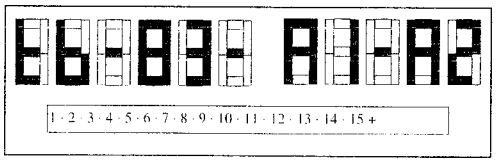
During the display test, different patterns will be shown on the local display of the DVD player. The user needs to step through these patterns using the PLAY key on the local keyboard. If any of the displayed patterns is incorrect, the display test has failed, and also the player test has failed.
The test patterns on display will be repeated in a loop (stepped through using PLAY) until the user presses NEXT on the local keyboard to proceed to the next test.

The LED Test

Next is the LED test; the LEDs on the DVD player are lit. Pressing PLAY will indicate that all LEDs are operational. To indicate that a LED did not light up, the user must press the PAUSE key. Pressing PLAY or PAUSE will proceed the user into the next test.

The Keyboard Test

During the keyboard test, the user needs to press all the keys on the local keyboard one by one. On the local display each key is represented by its scancode (a hexadecimal 2-digit code identifying the key to the DVD player).
Pressing a key will show its representing code on the local display of the DVD player: the first hexadecimal digit identifies the key pressed, the second indicates how many times this particular key was detected. In case the key is pressed more than once, the scancode is displayed as many times, with the second digit of its code increased each time. The display of scancodes scrolls from right to left, with the most recent scancode at the right. The following example gives a possible layout of the local display during the display/remote control test:



CL 96532097_004.eps
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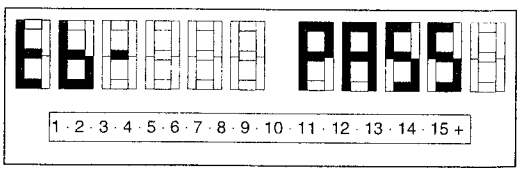
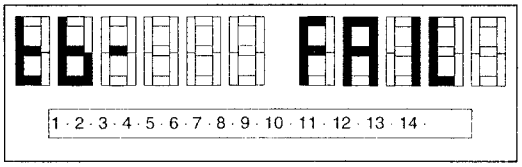
To terminate the keyboard test, press the NEXT key on the local keyboard of the DVD player and keep it pressed for 1 (one) full second. The keyboard test will terminate with a message on the local display. In case the keyboard test was successful, the message is:



CL 96532097_007.eps
130999

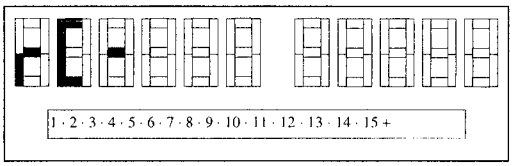
In case the keyboard test was not successful, the message will be:



CL 96532097_008.eps
130999

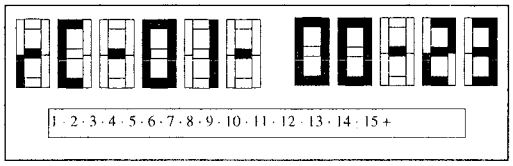
If the "tbFAIL"-message is displayed, the player test has failed. This is the end of the player test: turn off the DVD player, or press NEXT on the local keyboard of the DVD player to proceed to the next test.

The remote control test
For the remote control test, the user must press a key (any key) on the DVD's remote control. The display at the start of the test looks as follows:



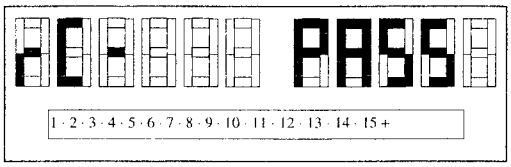
CL 96532111_032.eps
071099

When a remote control code has been received, its scancode is displayed as follows:



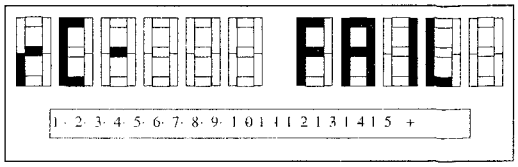
CL 96532097_009.eps
130999

The NEXT key can be pressed to exit this test.
However, if the user requires to test all keys on the remote control, (s)he can continue to press keys and these will all be displayed on the local display. With a code-table at hand this test can be used to test the full functionality of the DVD's remote control.
When the user has pressed NEXT on the local keyboard (NOT on the remote control!), the result of the remote control test is shown on the local display as follows:



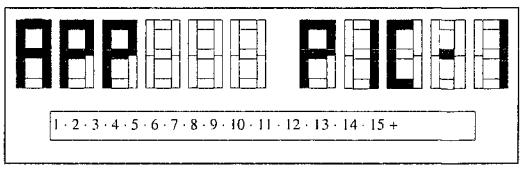
CL 96532097_011.eps
130999

in case of succes;



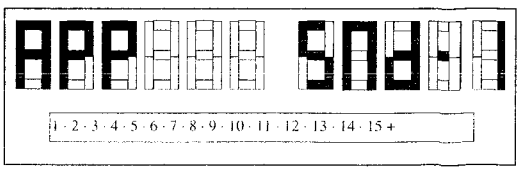
CL 96532097_012.eps
130999

if the test fails.
Pressing NEXT on the local keyboard again will proceed to the next test.
2. Testing the Monoboard
The picture tests involve putting a predefined picture on the connected television set, and asking the user for confirmation. When the picture has been put on screen, the local display asks for confirmation by the user as follows:



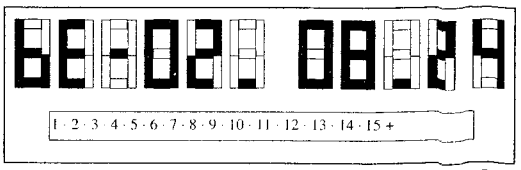
CL 96532097_013.eps
130999

If the user presses PLAY, he confirms the test; pressing PAUSE will indicate a fault in the test. At this time, the player test had failed and the DVD player can be switched off, or the user can proceed to the next test by pressing NEXT on the local keyboard of the DVD player.
Pressing the NEXT key on the local keyboard will start the next picture test (Colour set-up functional test).
When the picture tests are finished, the sound tests are run. A predefined sound will be generated, and again the user is asked to confirm this. The local display looks as follows:



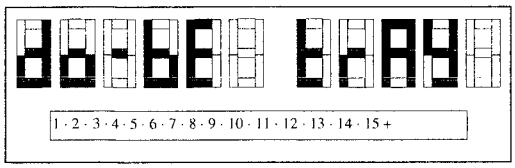
CL 96532097_014.eps
130999

Pressing PLAY confirms the test, PAUSE indicates test failure. If the test is faulty, the player test failed and the DVD player can be shut off. Subsequent sound tests will be numbered in ascending order.
Pressing NEXT on the local keyboard of the DVD player will take the user into the next test.
3. Testing the Basic Engine
Most tests on the basic engine require user interaction.
When the basic engine tests are started, the version of the basic engine which is present in the DVD player is shown on the local display, as follows:



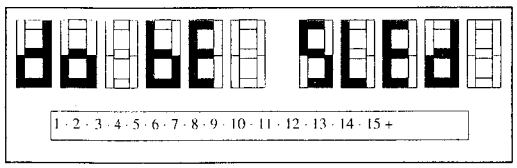
CL 96532097_015.eps
130999

The version number is displayed in decimal representation (the underscore replacing the dot). When the user presses NEXT on the local keyboard, the tests on the basic engine are started. First, the tray operation is tested. The user can move the tray in and out by pressing the PLAY or PAUSE key on the local keyboard (both keys have essentially the same function). The results need to be checked visually by the user, the software cannot detect any faults. The local display looks as follows:



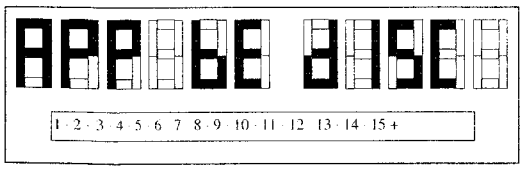
CL 96532097_016.eps
130999

To indicate this is a test of which the result is to be checked by the user, the first word on the local display is "do".
Except for testing the tray, this test is also meant to give the user the opportunity to put a disc into the DVD player for subsequent basic engine tests. Some of the following tests need a disc in the DVD player to operate properly. Always put a disc into the DVD player during this test! At the end of the basic engine tests there is opportunity to remove it (before the looptests start). Pressing the NEXT key on the local keyboard proceeds to the next test.
Second test is the sledge test; the user is asked to move the sledge by using the keys PLAY and PAUSE on the local keyboard (both keys have essentially the same function). This test needs to be checked visually by the user; the software cannot detect any faults. The local display during this test looks as follows:



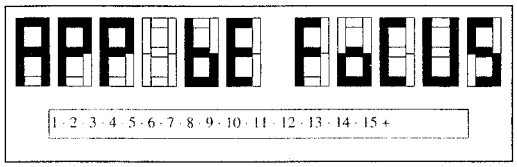
CL96532097_017.eps
130999

After pressing NEXT on the local keyboard the discmotor is tested; the local display looks as follows:



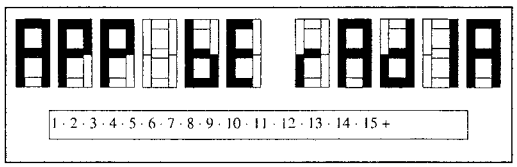
CL 96532097_018.eps
130999

The user is required to listen if the disc motor is running; this must be confirmed by pressing PLAY on the local keyboard. The PAUSE key is used to indicate the discmotor does not run. Pressing NEXT on the local keyboard starts the focus test. The local display looks as follows during this test:



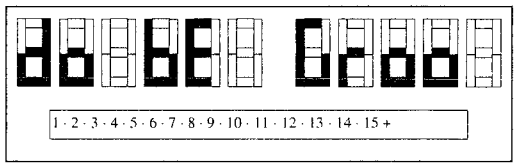
CL 96532097_019.eps
130999

By pressing PLAY the user confirms successful focussing by the basic engine; pressing PAUSE indicates a fault in the focus function.
Pressing NEXT on the local keyboard starts the radial function; the local display looks as follows:



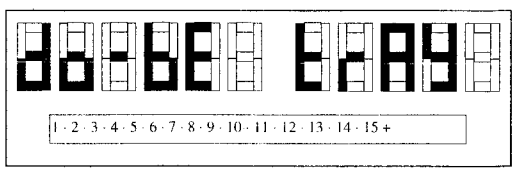
CL 96532097_020.eps
130999

Again, PLAY confirms the result, PAUSE indicates an error.
After pressing NEXT on the local keyboard, the grooves/jump test is started. As this is also a test that cannot be checked by the software, the user needs to perform a visual test. The local display looks as follows:



CL 96532097_021.eps
130999

By pressing PLAY the next grooves/jump position is taken; pressing PAUSE will go to the previous grooves/jump position. Switching through the different positions is done in a cyclic manner.
Press the NEXT key on the local keyboard to proceed to the last basic engine test: again, the tray is tested. This has been done at the beginning of the basic engine test already, the repeat is only meant to enable the user to remove the disc in the tray before proceeding. The local display will look as follows:



CL 96532097_016.eps
130999

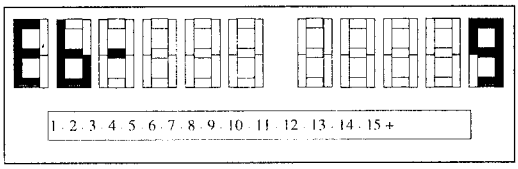
Press PLAY or PAUSE to operate the tray; remove the disc in the tray.
The tray will be closed automatically (if needed) before proceeding to the next tests (by pressing NEXT on the local keyboard).
Read Error Log

The contents of the error log will be displayed on the local display, as follows :

Note: This is an example only; no actual errorcode is intended

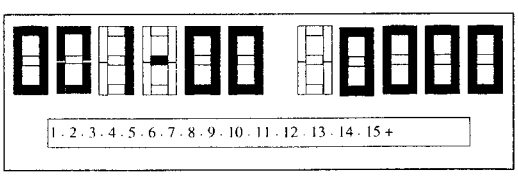
CL 96532097_022.eps
130999

The first two characters on the local display ("EL") indicate that the read-out mode of the error log is activated. After the hyphen 8 hexadecimal digits (one faultcode) are displayed. Below the row of 7-segment displays the highlighted number indicates the number of the faultcode being displayed. (Not for DVDv2B) The highest number indicates the oldest faultcode.
If, in the future, more than 15 faultcodes need to be displayed, the "+" character can be used to indicate the display of a faultcode in the range 16 - 30.
To step through the different fault codes, the PLAY (next) and PAUSE (previous) key on the local keyboard can be used. The display of faultcodes is cyclic. If the error log does not contain any fault codes, all displayed error codes will be "000 00000".
To switch off the display of the error log, the NEXT key must be pressed on the local keyboard.
Read Error Bits
The error bits are used to indicate that an error occurred once or more times; if that is the case the bit representing the error is set. To read out this field of error bits, the local display is used. Only the numbers of the errors where the bit is set will be displayed on the local display. The layout of the local display is (globally) as follows2:



CL 96532097_023.eps
130999

The number of the set bits is displayed in a cyclic manner.
Scrolling through the set error bits can be done with the PLAY key for 'next' and PAUSE key for 'previous'. Pressing the PLAY key at the last bit number will display the first bit number again, pressing the PAUSE button at the first bit number will display the last bit number in the list. The representation of bit numbers is decimal.
If no error bits are set, the number on the right side of the display will be "00"
Module Looptest
The module looptest is an infinite loop in which a number of nuclei are executed over and over again. The nuclei run are the same as in the dealer test; user interaction is not required.
During this looptest, the display looks as follows3:



CL 96532097_025.eps
130999

The leftmost three digits indicate which of the DVD player's modules is faulty; the explanation is in the following table:

Displayed Value	Indication for each module		
	Loader	Mono-board	Display PCB
000	ok	ok	ok
001	ok	ok	faulty
010	ok	faulty	ok
011	ok	faulty	faulty
100	faulty	ok	ok
101	faulty	ok	faulty
110	faulty	faulty	ok
111	faulty	faulty	faulty

CL 06532065_052.eps
230500

After the hyphen the (decimal) number indicates the number of times the looptest was performed.
The right side of the display shows an error code DNER (in decimal representation), which is built from a nucleus number (DN) and an error number (ER). This code indicates the last nucleus that returned an error code. For explanation of this DNER code, see document [SDD_DN].
Pressing NEXT on the local keyboard of the DVD player will exit this loop and show the end result of the player test.
End result of the player test is equal to the last display shown above: it shows which module is faulty and which nucleus caused the last error, as well as how many loops were performed.

Termination
To terminate the player test, switch off the DVD player.

5.11 Download Interfaces (not for service)

The download interface enables the user to download another version of diagnostic software into the RAM of the DVD player. The downloaded software will overrule the software which is placed in the DVD player's ROM; running the original diagnostic software is disabled until the DVD player is switched off and on again.
For download of diagnostic software, the RS232 port may be used.

5.11.1 Set-up physical interface components

Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm in Windows95) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity 1 stop bit and no flow control.
The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

5.11.2 Activation

Switch the DVD player on and the following text will appear on the screen of the terminal (emulation program):

```
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@ D <-
DVD diagnostic software awaiting download...@
```

CL06532065_035.eps
180500

The DVD player is now in a wait-mode, awaiting the download of a file in Motorola S3-format.
Enter the download command (which will be an "upload" from the terminal!) at the terminal:

```
upload <file>
```

CL96532111_028.eps
071099

Progress seen by the diagnostic software is indicated by displaying the character "*" on screen repeatedly; if the download software encounters an error, the end of the downloaded file will be awaited and instead of the "*"-character, the "+"- character will be used to indicate (erroneous) progress.
When download is finished, the following message will come from the DVD player:

```
Download succesful
Press return to start downloaded program...
```

CL96532111_029.eps
071099

When the user then presses a key, the DVD player will report

```
DVD Diagnostic Software version X.X
```

CL96532111_030.eps
071099

and start to run the downloaded software.
Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.
Note2 : For players without DRAM, the DRAM-tests will be scipped.

5.11.3 Usage

The usage of the downloaded software depends on the contents of that software and cannot be described here.

5.11.4 Termination (not for service)

To exit the download-interface and remove the downloaded software from the DVD player, switch off the DVD player.

External Scripts
A script is a sequence of nucleus calls. Internal scripts (e.g. scripts built into the diagnostic software itself) are in the form of a C-language module. However it cannot be expected from a customer to write C-modules in order to create new scripts.

The scripts that can be made externally are therefor in one of the following two forms:

1. A Procomm or Telex script Procomm or Telex can be used to write diagnostic scripts. The script language of both communication packages contains possibilities for construction of loops and branches in the scripts. Commands then going over the line will be exactly the same as described in the chapter "Command Interface". The diagnostic software (the engine) will receive normal RS232 commands and processes these as defined, sending results of these nuclei back over the RS232 line. In the Terminal the Procomm or Telex script determines which command sequence is followed
2. An Asterix-script Asterix-scripts are C-programs in which commands are sent to the diagnostic software (the engine). The construction of branches and loops is again located in the remote machine, i.e. the Asterix machine. Commands going over the line will be exactly the same as described in the chapter "Command Interface". The diagnostic software (the engine) will receive normal RS232 commands and processes these as defined, sending results of the called nuclei back over the RS232 line. In the Asterix PC the C-program determines which command sequence is followed.

Layout of menus and submenus for the Service Terminal
NOTE: a symbol "-->" in the next menu layouts indicates that that specific menu choice will invoke the display of a submenu. This symbol will also be used in the implementation of the menus (i.e. the "-->" will also appear in the user interface).

Main Menu

MAIN MENU
1. Audio -->
2. Basic Engine -->
3. Display PWB -->
4. Processor & Peripherals -->
5. Karaoke -->
6. Log -->
7. Miscellaneous -->
8. Video -->

First Level Submenus

AUDIO MENU
1. Deemphasis -->
2. Mute -->
3. PinkNoise -->
4. SineWave -->

BASIC ENGINE MENU
1. Disc Motor -->
2. Focus -->
3. Grooves -->
4. Radial -->
5. Reset [44]
6. Sledge -->
7. Tray -->
8. Version [37]

DISPLAY PWB MENU
1. Display [30]
2. Keyboard [27]
3. LEDs [29]
4. Remote control [28]
5. Version [28]

LOG MENU
1. Read last errors [31]
2. Read error bits [32]

3. Reset [33]

PROCESSOR AND PERIPHERALS MENU
1. Clock -->
2. DRAM Write/Read [9]
3. Flash -->
4. I2C -->
5. S2B -->
6. SDRAM Write/Read [16]

MISCELLANEOUS MENU
1. NVRam Utils -->
2. PalNtsc Line --> (Not for DVDv2B)
3. 2B Utils -->
4. Statistics Info -->
5. Read Application Version [46]

VIDEO MENU
1. Colourbar -->
2. Scart -->

KARAOKE MENU
1. Karaoke Mode Off [48a]
2. Karaoke Mode On [48b]
3. KaraokeMicInput [49]
4. KaraokeKey On [50a]
5. KaraokeKey Off [50b]
6. Karaoke Echo On [51a]
7. Karaoke Echo Off [51b]

Second level submenus

DEEMPHASIS MENU
1. Deemphasis 0 On [18a]
2. Deemphasis 0 Off [18b]
3. Deemphasis 1 On [18c]
4. Deemphasis 1 Off [18d]

for DVDv2B:
1. Deemphasis On [18a]
2. Deemphasis Off [18b]
3. Deemp 0 Tristate On [18e]
4. Deemp 0 Tristate Off [18f]
5. Deemp 1 Tristate On [18g]
6. Deemp 1 Tristate Off [18h]

MUTE MENU
1. Mute On [19a]
2. Mute Off [19b]

PINKNOISE MENU
1. Pinknoise On [20a]
2. Pinknoise Off [20b]

SINEWAVE MENU
1. Audio Sine On [21a]
2. Audio Burst On [21b]

DISC MOTOR MENU
1. Disc Motor On [39a]
2. Disc Motor Off [39b]

FOCUS MENU
1. Focus On [38a]
2. Focus Off [38b]

GROOVES MENU
1. Jump Grooves to Inside [42a]
2. Jump Grooves to Middle [42b]
3. Jump Grooves to Outside [42c]

RADIAL MENU
1. Radial Control On [40a]
2. Radial Control Off [40b]

SLEDGE MENU
1. Sledge Inwards [41a]
2. Sledge Outwards [41b]

TRAY MENU
1. Open Tray [43b]
2. Close Tray [43a]

LASER MENU
1. Laser Cd On[58a]
2. Laser Cd Off[58b]
3. Laser DVD On[58c]
4. Laser DVD Off[58d]

UCLOCK MENU
1. µClock A_CLK in CDDA Mode [7a]
2. µClock A_CLK in DVD Mode [7b]

FLASH MENU
1. Checksum FLASH [6]
2. Flash write access [10]

I2C MENU
1. I2C NVRAM Access [11]
2. I2C Display PWB [12]

S2B MENU
1. S2B Echo [13]
2. S2B Pass-through [14]

NVRAM MENU
1. NVRAM Config [34]
2. NVRAM reset [35]
3. NVRAM Mod [36]
4. NVRAM write/read [15]

PAL/NTSC MENU (Not for DVDv2B)
1. PalNtscHi [45a]
2. PalNtscLo [45b]

2B UTILS MENU
1. I2C Scart Check [54]
2. Scart to DVD [55a]
3. Scart Pass through [55b]
4. VideoColSetupI2C [52]
5. VideoColSetupHi [53a]
6. VideoColSetupLo [53b]

VIDEO COLOURBAR MENU
1. Colourbar DENC On [23a]
2. Colourbar DENC Off [23b]

SCART MENU
1. Scart Low [25a]
2. Scart Medium [25b]
3. Scart High [25c]

STATISTICS INFO MENU
1. Total Nr of Times Tray Open [47a]
2. Toat Time Power On [47b]
3. Total Play-time CDDA & VCD [47c]
4. Total Play-time DVD [47d]

Screen layout with menus

When menus are used, no specific screen layout can be given: menu information will not be in a special format, except for the layout as mentioned in the previous paragraphs.
A typical menu session can look as follows:

```
----------< top of screen >----------
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK
(M)enu, (C)ommand, (S)2B-interface or (D)ownload? [M]:@
M <--

MAIN MENU
1. Audio -->
2. Basic Engine -->
3. Display PWB -->
4. Processor & Peripherals -->
5. Karaoke -->
6. Log -->
7. Miscellaneous -->
8. Video -->
Select> 4 <--

PROCESSOR AND PERIPHERALS MENU
1. Clock -->
2. DRAM Write/Read [9]
3. Flash -->
4. I2C -->
5. S2B -->
6. SDRAM Write/Read [16]
Select> 6 <--
----------< bottom of screen >----------
```

Depending on the height of the screen, the text will start scrolling off the top of the screen.

Layout of Results diagnostic nuclei on control/service PC

Results returned from a Diagnostic Nucleus to the control/ service PC will have a maximum length of 300 characters and are terminated by a CR character (included in the string length)
The result has the following layout
< number >< string > [OK I ER] @< CR >
The use of the "@" enables the Asterix system on the Control PC to parse the output string of each nucleus into a database.
< number > is a 4-digit decimal number padded with leading zeros if its value is less than 4 digits. The first two digits identify the generating nucleus (or goup of nuclei), the latter two digits indicate the error number.
< string > is a text string containing information about the result of the Diagnostic Nucleus.
< number > and < string > are defined in [SDD_DN] in the output sections of each Nucleus.
Examples:

```
1. 0001 Unknown command ER @
2. 3100 OK @
3. 0901 Data line X is not connected to the DRAM ER @
```

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071099

5.12 Diagnostic Nuclei

Each nucleus contains an atomic and independent diagnostic test, testing a functional part of the DVD player hardware on component level. Each Nucleus returns a result message to its caller. Some tests (e.g. generating a colour bar) can only return an "OK" result. Internal communication will be done via a uniform interface between the diagnostic Engine, Scripts and the Diagnostic Nuclei.
The diagnostic Engine can only operate if a certain (minimal) set of hardware is functioning properly. To test this set of hardware, a set of basic diagnostic nuclei is embedded in the DVD player. Each basic diagnostic nucleus will only test that part of the hardware which is required for execution of the diagnostic Engine, e.g. a RAM test will only test that part of RAM that is used by the diagnostic engine. After the Diagnostic Engine is operational it is possible to do a full RAM diagnostic. All basic diagnostic nuclei start with prefix 'Basic'.
In the overview each Diagnostic Nucleus consists of a reference number, a reference name and remarks. Reference number and name are coupled and one of them is enough for unique identification. The reference number can be used to find the description of the Diagnostic Nucleus in paragraph Error! Reference source not found..# where # is the reference number.

5.12.1 Basic Diagnostic Nuclei

Ref.	Reference Name	Remark
1	BasicSpAcc	Serial port Access test/ initialisation
2a	BasicInterconDram	Data and address bus Interconnection (only for DVDv2A)
2b	BasicInterconSdram	Data and address bus interconnection
3	BasicDramWrR	DRAM Write Read (only for DVDv2A)
4	BasicSdramWrR	SDRAM Write Read
5	BasicSramWrR	SRAM Write Read

5.12.2 Processor and Peripherals

Ref.	Reference Name	Remark
6	PapChksFl	Checksum FLASH
7a	PapUclkAclkCdda	uClock A_CLK in CD-DA mode
7b	PapUclkAclkDvd	uClock A_CLK in DVD mode
9	PapDramWrR	DRAM Write Read (only for DVDv2A)
10	PapFlashWrAcc	FLASH Write Access
11	PapI2cNvram	I2C NVRAM access
12	PapI2cDisp	I2C Display PWB
13	PapS2bEcho	S2B Echo
14	PapS2bPass	S2B Pass-through
15	PapNvramWrR	NVRAM Write Read

5.12.3 Components

Ref. #	Reference Name	Remark
16	CompSdramWrR	SDRAM Write Read

5.12.4 Audio

Ref.	Reference Name	Remark
17	AudioSig	Audio Signature (Optional)
18a	AudioDeemp0On	Audio De-emphasis 0 On
	AudioDeempOn (DVD2B)	Audio De-emphasis On (DVDv2B)
18b	AudioDeemp0Off	Audio De-emphasis 0 Off
	AudioDeempOff (DVD2B)	Audio De-emphasis Off (DVDv2B)
18c	AudioDeemp1On	Audio De-emphasis 1 On (Not for DVDv2B)
18d	AudioDeemp1Off	Audio De-emphasis 1 Off (Not for DVDv2B)
18e	AudioDeemp0TristateOn	Audio De-emphasis 0 in tristate/bidirectional mode (DVDv2B)
18f	AudioDeemp0TristateOff	Audio De-emphasis 0 back in output mode (Off) (DVDv2B)
18g	AudioDeemp1TristateOn	Audio De-emphasis 1 in tristate/bidirectional mode (DVDv2B)
18h	AudioDeemp1TristateOff	Audio De-emphasis 1 back in output mode (Off) (DVDv2B)
19a	AudioMuteOn	Audio Mute On
19b	AudioMuteOff	Audio Mute Off
20a	AudioPinkNoiseOn	Audio Pinknoise On
20b	AudioPinkNoiseOff	Audio Pinknoise Off
21a	AudioSineOn	Audio Sine signal On/Off
21b	AudioSineBurst	Audio Sine signal Burst
56a	AudioDeemp0On	PIO-pins as used in 2A for Deemphasis
56b	AudioDeemp0Off	PIO-pins as used in 2A for Deemphasis
56c	AudioDeemp1On	PIO-pins as used in 2A for Deemphasis
56d	AudioDeemp1Off	PIO-pins as used in 2A for Deemphasis

5.12.5 Video

Ref.	Reference Name	Remark
23a	VideoColDencOn	Colourbar DENC On
23b	VideoColDencOff	Colourbar DENC Off
25a	VideoScartLo	Scart Low
25b	VideoScartMi	Scart Medium
25c	VideoScartHi	Scart High
52	VideoColSetupCom	Colour Setup Communication
53a	VideoColSetupHi	Colour Setup High
53b	VideoColSetupLo	Colour Setup Low
54	VideoScartSwCom m	Scart Switch communication
55a	VideoScartSwDvd	Scart Switch Dvd
55b	VideoScartSwPass	Scart Switch Pass-through

Ref.	Reference Name	Remark
57a	VideoScartPinLo	PIO-pins as used in 2A for Scart-switching
57b	VideoScartPinMi	PIO-pins as used in 2A for Scart-switching
57c	VideoScartPinHi	PIO-pins as used in 2A for Scart-switching

5.12.6 DisplayPWB (slave processor)

Ref.	Reference Name	Remark
26	DispVer	Version number
27	DispKeyb	Keyboard
28	DispRc	Remote Control
29	DispLed	LEDs
30	DispDisplay	Display

5.12.7 Log (error logging in NVRAM)

Ref.	Reference Name	Remark
31	LogReadErr	Read last Errors
32	LogReadBits	Read errors Bits
33	LogReset	Reset

5.12.8 Miscellaneous

Ref.	Reference Name	Remark
34	MiscReadConfig	Read Configuration area from NVRAM
35	MiscNvramReset	NVRAM Reset
36	MiscNvramMod	Modify NVRAM contents
45a	MiscPalNtscHi	Check if PAL/NTSC line is high (Not for DVDv2B)
45b	MiscPalNtscLo	Check if PAL/NTSC line is low (Not for DVDv2B)
46	MiscApplVer	Read version of application software
47a	MiscTrayOpenNr	Read the number of times the tray opened
47b	MiscPowerOnTime	Read the total time the player's power has been on
47c	MiscPlayTimeCddaVcd	Read the Playtime of CDDA and VCD discs
47d	MiscPlayTimeDvd	Read the Playtime of DVD discs

5.12.9 Basic Engine

Ref.	Reference Name	Remark
37	BeVer	Version number
38a	BeFocusOn	Focus On
38b	BeFocusOff	Focus Off
39a	BeDiscmotorOn	Discmotor On
39b	BeDiscmotorOff	Discmotor Off
40a	BeRadialOn	Radial control On
40b	BeRadialOff	Radial control Off
41a	BeSledgeIn	Sledge Inwards
41b	BeSledgeOut	Sledge Outwards
42a	BeGroovesIn	jump Grooves to Inside
42b	BeGroovesMid	jump Grooves to Middle
42c	BeGroovesOut	jump Grooves to Outside
43a	BeTrayIn	Tray In
43b	BeTrayOut	Tray Out
44	BeReset	Reset Basic Engine
58a	LaserCdOn	CD Laser on
58b	LaserCdOff	CD Laser off
58c	LaserDvdOn	DVD Laser on
58d	LaserDvdOff	DVD Laser off

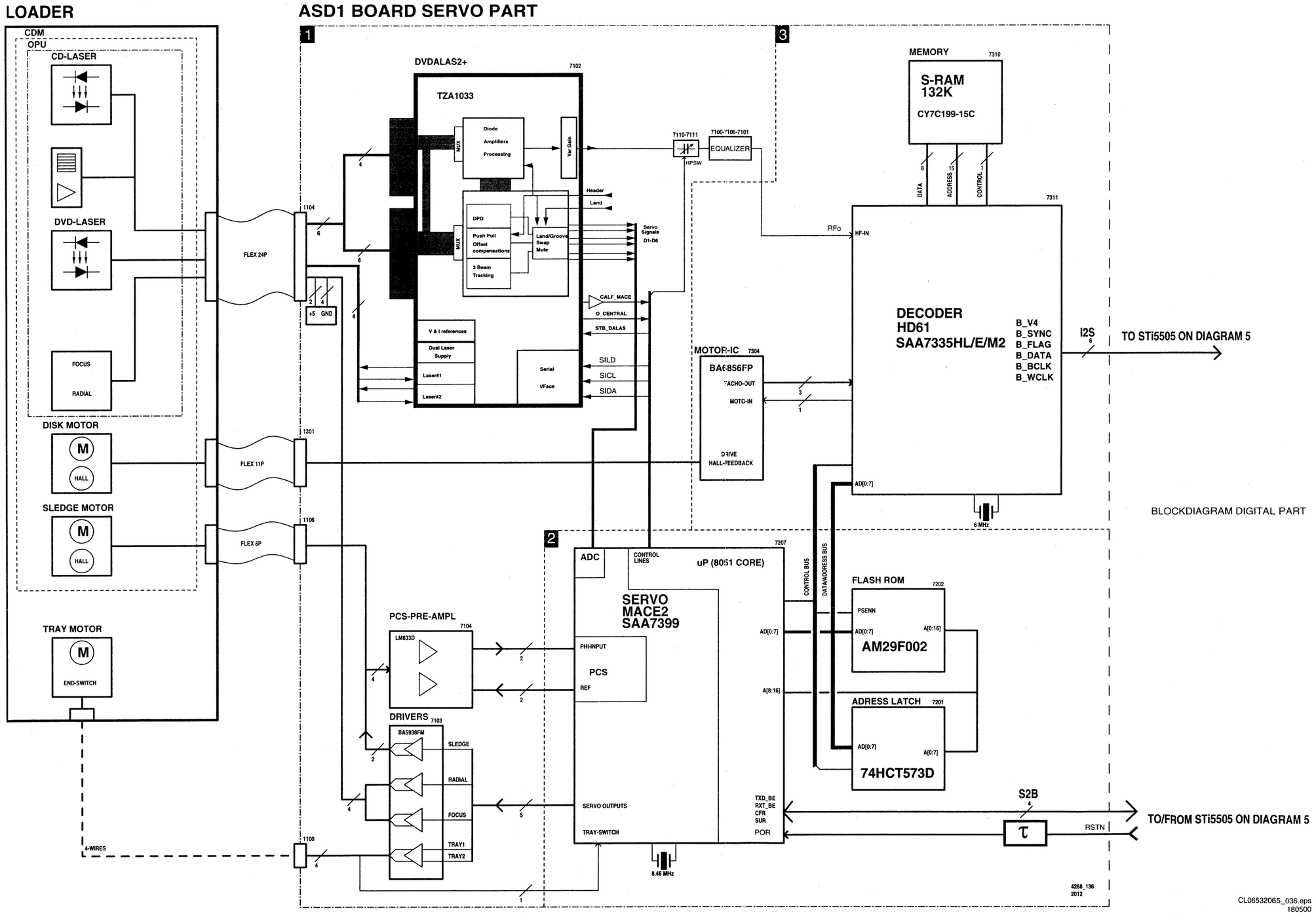
5.12.10 Karaoke

Ref.	Reference Name	Remark
48a	KaraokeModeOff	Switch Karaoke mode off
48b	KaraokeModeOn	Switch Karaoke mode on
49	KaraokeMicInput	Check path from the microphone input to audio output
50a	KaraokeKeyOn	Set Karaoke Key to the maximum level (1200 cent)
50b	KaraokeKeyOff	Set Karaoke Key to flat octave (0 cent)
51a	KaraokeEchoOn	Set Echo Control fuction on
51b	KaraokeEchoOff	Set Echo Control function off

Note: A new Compair version for repair of the MONO boards will be developed.

6. Block diagrams

Servo



BLOCKDIAGRAM DIGITAL PART

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180500

Didital

ASD1 BOARD DIGITAL PART

5

6

4

RSTN

S2B

TO /FROM MACE2 (DIAGRAM 2)

FROM HD61 DECODER (DIAGRAM 3)

I2S

B_V4
B_WCLK
B_DATA
B_BCLK
B_FLAG
B_SYNC

TXD_BE
RXD_BE
CFR
SUR

7503

UART

UART

FRONT END INTERFACE

OSD

PROGRAMMABLE I/O

AUDIO DECODER

AUDIO

DEMULTIPLEXER

VIDEO

MPEG DECODER

VIDEO ENCODER

SUBPICTURE

HOST ST20

STi5505

MEMORY INTERFACE

SDRAM CONTROLLER

I2C CONTROLLER

SERVICE

SCART[0:1]

MUTE

SCLK
PCM_OUT0
LRCLK
SPDIF_OUT

PCM_CLK

R_OUT
G_OUT
B_OUT
C_OUT
CVBS_OUT
Y_OUT

SEL_ACLK

SDA
SCLK

I2C

RESETN

STB_CONT

SYSTEM DATA BUS

SYSTEM ADDRESS BUS

SYSTEM CONTROL BUS

SDRAM INTERFACE

7504

27 MHz

7505

EEPROM
ST24E32M6

7401

16Mb FLASH
AM29LV160BT

7404

16Mb SDRAM
MT48LC1M16A1TG -7S

7405

16Mb SDRAM
MT48LC1M16A1TG-7S

TXD_SER
RXD_SER
RTS_SER
CTS_SER

7600

CONN. 1602

SERVICE SERIAL INTERFACE

SERVICE

CONN. 1603

DEEM[0:1]

7604, 7607

SCART 0/6/12V

0_6_12V

7608,7609,7610

MUTE

MUTE_AV

BCLK
DATA
WCLK

TO/FROM A/V-MUX BOARD

PCM (3X) DIG. OUT

7611

3V3
5V

DIG_OUT

ACLK

CVBS
RGB
S-VHS

7612-7618

VIDEO FILTER BUFFER

R/C
G
B/CVBS
CVBS/Y

P50

+5V

-5V

PCM__CLK

7616

CLOCK SYNTHESIZER
MK2742

CONN. 1604

Y - C

+3V3
+6Vstby
+12Vstby
-8Vstby
PCMout1
PCMout2
HSYNC

TO A/V-MUX BOARD

OPTION

CONN. 1600

+3V3
+5V
+5Vstby
-8Vstby
+6Vstby
+12Vstby

POWER SUPPLY

CONN. 1501

P50

STB_CONT

TO/FROM DISPLAY

4268_136
2012

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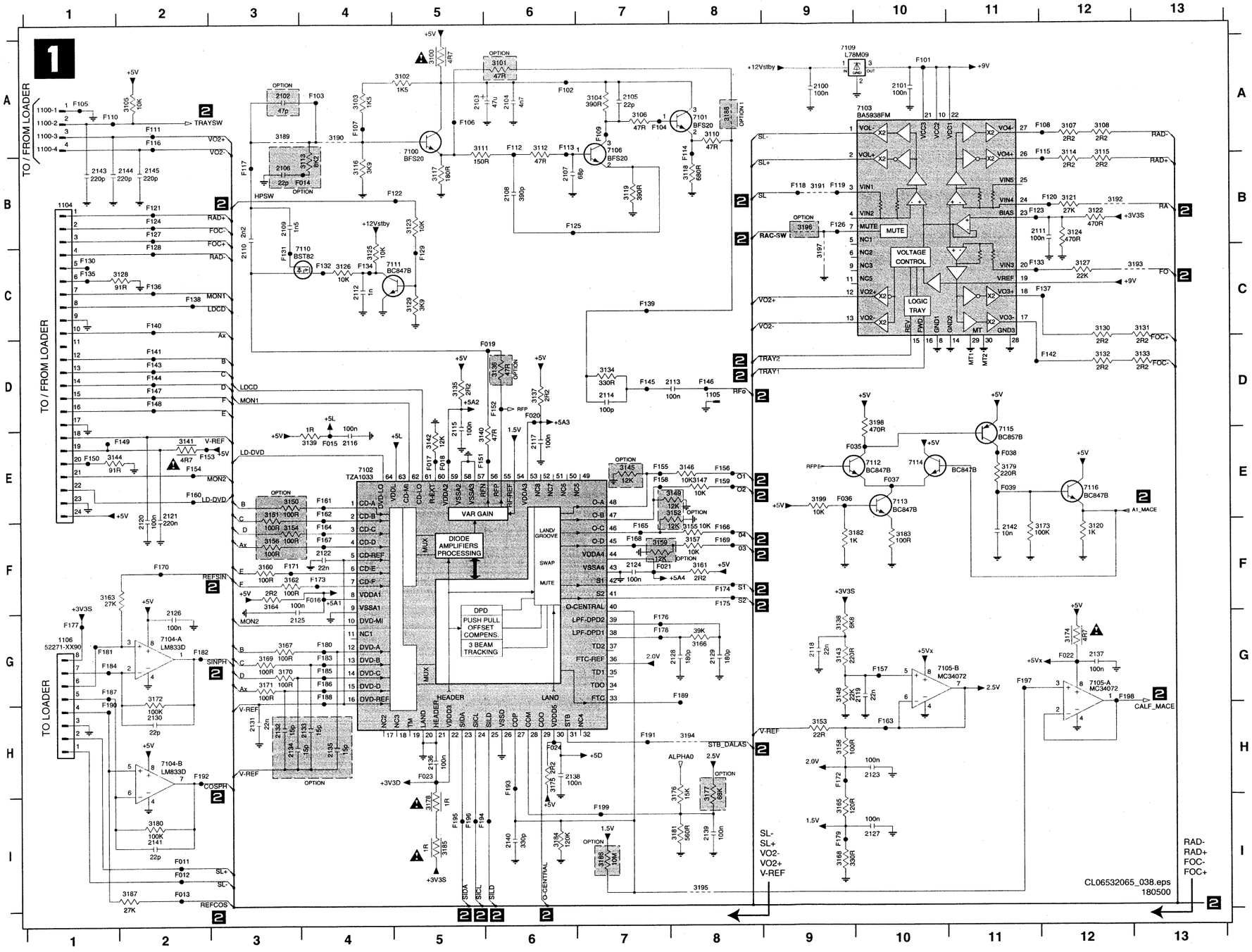
180500

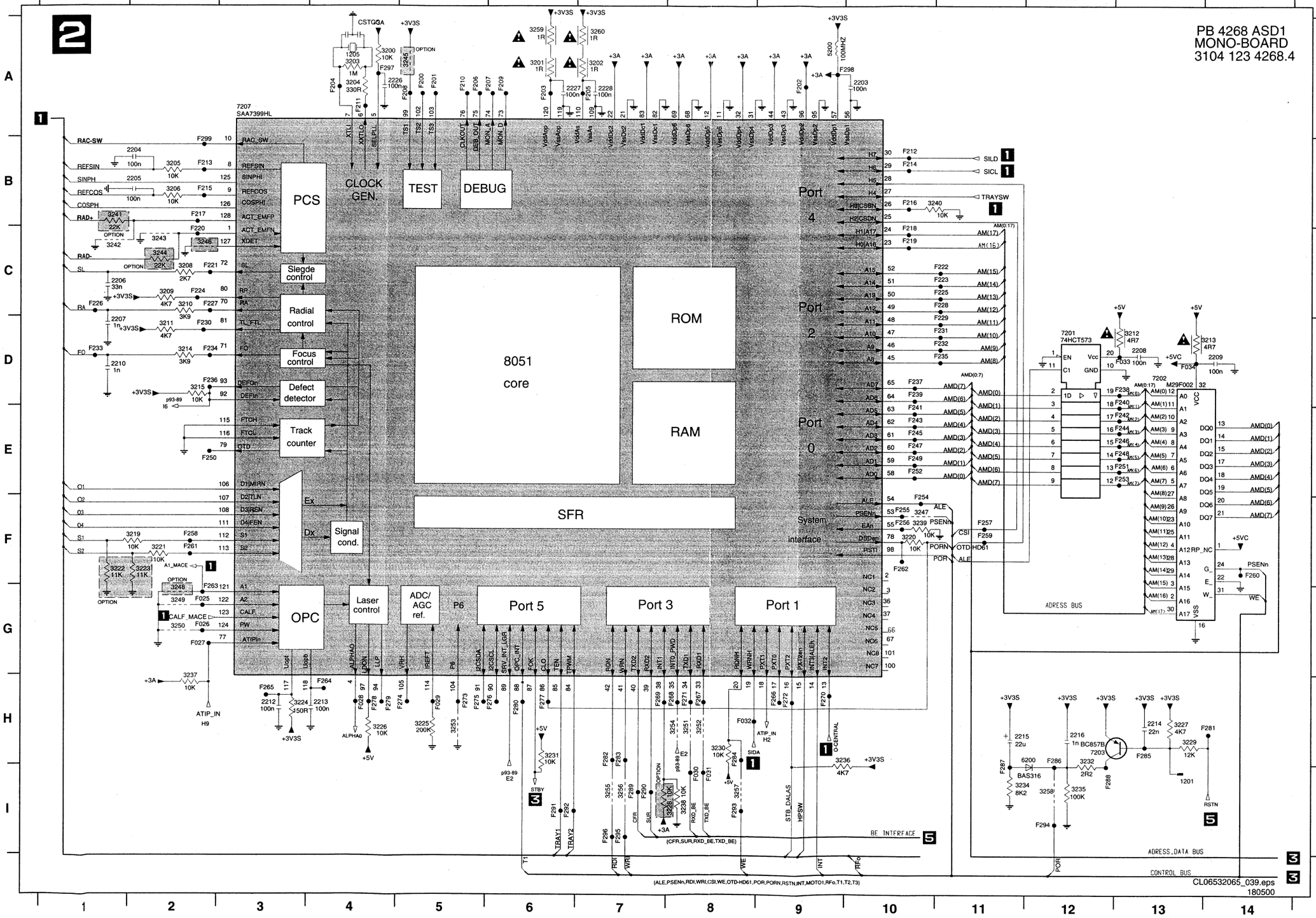
7. Electrical diagrams and PWB's

SERVO DALAS



1100-1 A1
1100-2 A1
1100-3 A1
1100-4 A1
1104 B1
1105 D8
1106 G1
2100 A9
2101 A10
2102 A3
2103 A5
2104 A6
2105 A7
2106 B3
2107 B6
2108 B6
2109 B3
2110 B3
2111 B11
2112 C4
2113 D8
2114 D7
2115 D5
2116 E4
2117 E6
2118 G9
2119 G10
2120 E2
2121 E2
2122 F4
2123 H10
2124 F7
2125 G3
2126 G2
2127 I10
2128 G8
2129 G8
2130 H2
2131 H3
2132 H3
2133 H4
2134 H3
2135 H4
2136 H5
2137 G12
2138 H6
2139 I8
2140 I6
2141 I2
2142 F11
2143 B1
2144 B2
2145 B2
3100 A5
3101 A6
3102 A5
3103 A4
3104 A7
3105 A2
3106 A7
3107 A12
3108 A12
3110 A8
3111 A5
3112 A6
3113 B4
3114 B12
3115 B12
3116 B4
3117 B5
3118 B8
3119 B7
3120 F12
3121 B12
3122 B12
3123 B5
3124 B12
3125 C4
3126 C4
3127 C12
3128 C2
3129 C5
3130 C12
3131 C13
3132 D12
3133 D13
3134 D7
3135 D5
3136 D6
3137 D6
3138 G9
3139 E4
3140 E5
3141 E2
3142 E5
3143 G9
3144 E1
3145 E7
3146 E8
3147 E8
3148 G9
3149 E8
3150 E3
3151 E3
3152 E8
3153 H9
3154 F3
3155 F8
3156 F3
3157 F8
3158 H9
3159 F7
3160 F3
3161 F8
3162 F3
3163 F1
3164 F3
3165 I9
3166 G8
3167 G3
3168 I9
3169 G3
3170 G3
3171 G3
3172 G2
3173 F12
3174 G12
3175 H6
3176 H8
3177 H8
3178 I5
3179 E11
3180 I2
3181 I8
3182 F10
3183 F10
3184 I6
3185 I5
3186 I7
3187 I2
3188 A8
3189 A3
3190 A4
3191 B9
3192 B12
3193 C13
3195 I8
3196 B9
3197 C9
3198 D10
3199 E9
7100 A5
7101 A8
7102 E4
7103 A10
7104-A G2
7104-B H2
7105-A G12
7105-B G10
7106 A7
7109 A9
7110 C4
7111 C5
7112 E10
7113 E10
7114 E10
7115 D11
7116 E12
F011 I2
F012 I2
F013 I2
F014 B4
F015 E4
F016 F4
F017 E5
F018 E5
F019 D6
F020 D6
F021 F7
F022 G12
F023 H5
F024 H6
F035 E9
F036 E9
F037 E10
F038 E11
F039 E11
F101 A10
F102 A6
F103 A4
F104 A7
F105 A1
F106 A5
F107 A4
F108 A12
F109 A7
F110 A1
F111 A2
F112 A6
F113 A6
F114 A8
F115 B12
F116 A2
F117 B3
F118 B9
F119 B9
F120 B12
F121 B2
F122 B5
F123 B11
F124 B2
F125 B6
F126 B9
F127 B2
F128 C2
F129 C5
F130 C1
F131 C3
F132 C4
F133 C11
F134 C4
F135 C1
F136 C2
F137 C12
F138 C2
F139 C7
F140 C2
F141 D2
F142 D12
F143 D2
F144 D2
F145 D7
F146 D8
F147 D2
F148 D2
F149 E2
F150 E1
F151 E5
F152 D6
F153 E2
F154 E2
F155 E7
F156 E8
F157 G10
F158 E7
F159 E8
F160 E2
F161 E4
F162 E4
F163 H10
F164 F4
F165 F7
F166 F8
F167 F4
F168 F7
F169 F8
F170 F2
F171 F3
F172 H9
F173 F4
F174 F8
F175 F8
F176 G7
F177 G1
F178 G7
F179 I9
F180 G4
F181 G1
F182 G2
F183 G4
F184 G1
F185 G4
F186 G4
F187 G1
F188 G4
F189 G8
F190 H1
F191 H7
F192 H2
F193 H6
F194 I5
F195 I5
F196 I5
F197 G11
F198 G12
F199 I7

SERVO MACE



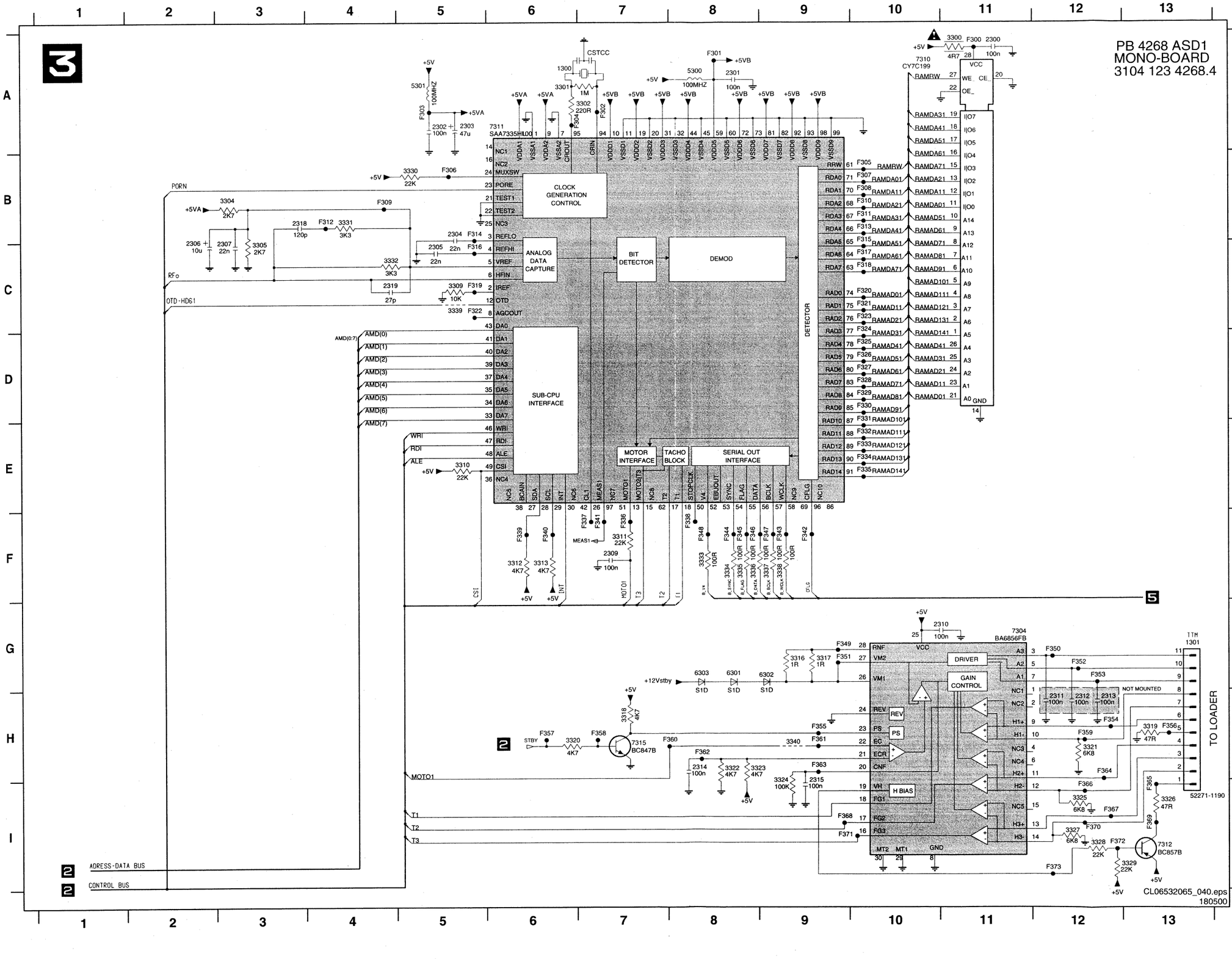
1201 I13	F228 C11
1205 A4	F229 D11
2203 A10	F230 D2
2204 B2	F231 D11
2205 B2	F232 D11
2206 C1	F233 D1
2207 D1	F234 D2
2208 D13	F235 D11
2209 D14	F236 D2
2210 D1	F237 D10
2212 H3	F238 D13
2213 H4	F239 D10
2214 H13	F240 D13
2215 H11	F241 E10
2216 H12	F242 E13
2226 A4	F243 E10
2227 A6	F244 E13
2228 A7	F245 E10
3200 A4	F246 E13
3201 A6	F247 E10
3202 A7	F248 E13
3203 A4	F249 E10
3204 A4	F250 E2
3205 B2	F251 E13
3206 B2	F252 E10
3208 C2	F253 E13
3209 C2	F254 F10
3210 C2	F255 F10
3211 D2	F256 F10
3212 D13	F257 F11
3213 D14	F258 F2
3214 D2	F259 F11
3215 D2	F260 F14
3219 F2	F261 F2
3220 F10	F262 F10
3221 F2	F263 G2
3222 F1	F264 H4
3223 F2	F265 H3
3224 H3	F266 H9
3225 H5	F267 H8
3226 H4	F268 H8
3227 H13	F269 H7
3228 I8	F270 H9
3229 H13	F271 H8
3230 H8	F272 H9
3231 H6	F273 H5
3232 H12	F274 H5
3234 I11	F275 H5
3235 I12	F276 H6
3236 H9	F277 H6
3237 H2	F278 H4
3238 I8	F279 H4
3239 F10	F280 H6
3240 B10	F281 H14
3241 B1	F282 H7
3242 C1	F283 H7
3243 C2	F284 H8
3244 C2	F285 H13
3245 A5	F286 H12
3246 C2	F287 I11
3247 F10	F288 I12
3248 G2	F289 I7
3249 G2	F290 I7
3250 G2	F291 I6
3251 H8	F292 I6
3252 H8	F293 I8
3253 H5	F294 I12
3254 H8	F295 I7
3255 I7	F296 I7
3256 I7	F297 A4
3257 I8	F298 A10
3258 I12	F299 B2
3259 A6	
3260 A7	
5200 A9	
6200 H12	
7201 D12	
7202 D13	
7203 H12	
7207 A3	
F025 G2	
F026 G2	
F027 G2	
F028 H4	
F029 H5	
F030 I8	
F031 I8	
F032 H8	
F033 D13	
F034 D13	
F200 A5	
F201 A5	
F202 A9	
F203 A6	
F204 A4	
F205 A7	
F206 A5	
F207 A6	
F208 A5	
F209 A6	
F210 A5	
F211 A4	
F212 B10	
F213 B2	
F214 B10	
F215 B2	
F216 B10	
F217 B2	
F218 C10	
F219 C10	
F220 C2	
F221 C2	
F222 C11	
F223 C11	
F224 C2	
F225 C11	
F226 C1	
F227 C2	

Decoder

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

CL06532065_040.eps
180500

1300 A6
1301 G13
2300 A11
2301 A8
2302 A5
2303 A5
2304 B5
2305 C5
2306 C2
2307 C3
2309 F7
2310 G11
2311 H12
2312 H12
2313 H12
2314 H8
2315 I9
2318 B3
2319 C4
3300 A11
3301 A6
3302 A7
3304 B3
3305 C3
3309 C5
3310 E5
3311 F7
3312 F6
3313 F6
3316 G9
3317 G9
3318 H7
3319 H13
3320 H6
3321 H12
3322 H8
3323 H8
3324 I9
3325 I12
3326 I13
3327 I12
3328 I12
3329 I13
3330 B5
3331 B4
3332 C4
3333 F8
3334 F8
3335 F8
3336 F8
3337 F9
3338 F9
3339 C5
3340 H9
5300 A8
5301 A5
6301 G8
6302 G9
6303 G8
7304 G11
7310 A10
7311 A6
7312 I13
7315 H7
F300 A11
F301 A8
F302 A7
F303 A5
F304 A6
F305 B10
F306 B5
F307 B10
F308 B10
F309 B4
F310 B10
F311 B10
F312 B4
F313 B10
F314 B5
F315 C10
F316 C5
F317 C10
F318 C10
F319 C5
F320 C10
F321 C10
F322 C5
F323 C10
F324 D10
F325 D10
F326 D10
F327 D10
F328 D10
F329 D10
F330 D10
F331 E10
F332 E10
F333 E10
F334 E10
F335 E10
F336 F7
F337 F7
F338 F8
F339 F6
F340 F6
F341 F7
F342 F9
F343 F9
F344 F8
F345 F8
F346 F8
F347 F9
F348 F8
F349 G9
F350 G12
F351 G9
F352 G12
F353 G12
F354 H12
F355 H9
F356 H13
F357 H12
F358 H7
F359 H12
F360 H8
F361 H9
F362 H8
F363 H9
F364 H12
F365 I13
F366 I12
F367 I12
F368 I9
F369 I13
F370 I12
F371 I9
F372 I12
F373 I12



Memory

4 MEMORY PART

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

OPTION = NOT USED FOR FUTURE APPLICATION: I²C FROM MASTER TO SLAVE FOR SYSTEMS / COMBI'S

SYSTEM DATA Bus 5
SYSTEM ADDRESS Bus 5
RAM/ROM Interface 5
SDRAM Interface 5

OPTION

+5Vstby, 5400 100MHZ, F421, +5V_DS, 2400 100n
7406 PCF8584T, VDD, 20
RESET_I2C, CE1, DTACK, IRQ_I2C, CLK_8MHz, SDA_EXE, SCL_EXE
RESET_ISTROBE_, CS_, A0, WR_, RD_, INT_|SCL-OUT, IACK_|SDA-IN, CLK, SDA|SDA-OUT, SCL|SCL-IN, VSS, 10
F422, F423, F424, F425, 3400 100R, 3401 100R
DB7 D7, DB6 D6, DB5 D5, DB4 D4, DB3 D3, DB2 D2, DB1 D1, DB0 D0
RWN, A1

OPTION

+5V_DS, +5V_DS, 2415 100n, 3402 10K
7400-A 74HCT00D 14, 1, 2, 3, 7
F406
7400-D 74HCT00D 14, 12, 13, 11, 7
3416 WAIT 5
7400-B 74HCT00D 14, 4, 5, 6, 7
5 CE1

OPTION

+5VOSC, 2416 100n, 2417 100n
7402 74HCT1G79 5, 1, 2, 3, 4
F430
7403 74HCT1G04 6, 2, 3, 1, 4, NC
5 AUXCLK, F431, 3407 22R
CLK_6MHz

VDD_MEM, 2405 100n
7401 Am29LV160BT 23, VCC
A0 11, A1 10, A2 9, A3 8, A4 7, A5 6, A6 5, A7 4, A8 42, A9 41, A10 40, A11 39, A12 38, A13 37, A14 36, A15 35, A16 34, A17 3, A18 2, A19 43, A20
DQ0 15, DQ1 17, DQ2 19, DQ3 21, DQ4 24, DQ5 26, DQ6 28, DQ7 30, DQ8 16, DQ9 18, DQ10 20, DQ11 22, DQ12 25, DQ13 27, DQ14 29, DQ15|A-1 31
3412, F434 OPTION, 3413, RWN, CE_ROM, FLASH_OEN
CE_, OE_, WE_, RESET_, BYTE_, VSS1 13, VSS2 32
3405 10K, F435 44, 1, 33
3414, 3415 OPTION, VDD_MEM
3416, F432, VDD_MEM, VDD_MEM

OPTION

3409, +5V_DS
5 27M_CLKIN, 7400-C 74HCT00D 14, 9, 8, 10, 2414 10n
3410, 3408 100R, F428, 27M_CLKOUT 5

VDD_MEM2
2401 100n, 2402 100n, 2406 100n, 2407 100n, 2410 100n, 2411 100n
7404 MT48LC1M16A1TG, 1, 25, 7, 13, 38, 44, BOTTOM
VDD, VDDQ
AD11 19 BA, AD0 21 A0, AD1 22 A1, AD2 23 A2, AD3 24 A3, AD4 27 A4, AD5 28 A5, AD6 29 A6, AD7 30 A7, AD8 31 A8, AD9 32 A9, AD10 20 A10
CLK 35 CLK, VDD_MEM2 3403 10K F415, 34 CKE, CSN 18 CS_, RASN 17 RAS_, CASN 16 CAS_, WEN 15 WE_, DQMU 36 DQMH, DQML 14 DQML
DQ0 2 DQ7, DQ1 3 DQ6, DQ2 5 DQ5, DQ3 6 DQ4, DQ4 8 DQ3, DQ5 9 DQ2, DQ6 11 DQ1, DQ7 12 DQ0, DQ8 39 DQ15, DQ9 40 DQ14, DQ10 42 DQ13, DQ11 43 DQ12, DQ12 45 DQ11, DQ13 46 DQ10, DQ14 48 DQ9, DQ15 49 DQ8
BANK SELECT, DATA INPUT REGISTER, I/O CONTROL, LWE, LDQM
ADDRESS REGISTER, ROW BUFFER REFRESH COUNTER, ROW DECODER, 512Kx16, 512Kx16, SENSE AMP, OUTPUT BUFFER
COLUMN DECODER, LATENCY & BURST LENGTH, PROGRAMMING REGISTER, TIMING REGISTER, COL. BUFFER
LRAS, LCBR, LCAS, LWE, LWCBR, LCKE, LQDM
NC 33, 37
VSS 26, 50, VSSQ 4, 10, 41, 47

7405 MT48LC1M16A1TG, TOP
2403 100n, 2404 100n, 2408 100n, 2409 100n, 2412 100n, 2413 100n
3404 10K F416, VDD_MEM2

+3V3, 5402 100MHZ, F419, VDD_MEM, 2418 100u
+3V3, 5403 100MHZ, F420, VDD_MEM2, 2419 47u, 2420 47u

2400 B3
2401 C9
2402 C10
2403 C12
2404 C13
2405 B6
2406 C9
2407 C10
2408 C12
2409 C13
2410 C9
2411 C10
2412 C12
2413 C13
2414 H7
2415 E1
2416 H2
2417 H3
2418 I10
2419 I13
2420 I13
3400 C1
3401 C2
3402 E1
3403 F8
3404 F11
3405 F5
3406 I7
3407 I3
3409 H7
3410 I6
3412 E5
3413 F5
3414 F5
3415 F5
3416 G5
3418 E4
5400 A3
5402 I9
5403 I12
7400-A E2
7400-B F2
7400-C I6
7400-D E3
7401 C6
7402 H2
7403 H3
7404 D9
7405 D12
7406 B3
F406 E2
F415 G8
F416 G11
F419 I10
F420 I13
F421 A3
F422 C2
F423 C2
F424 C2
F425 C2
F428 I8
F430 H2
F431 H1
F432 G5
F434 F5
F435 F5

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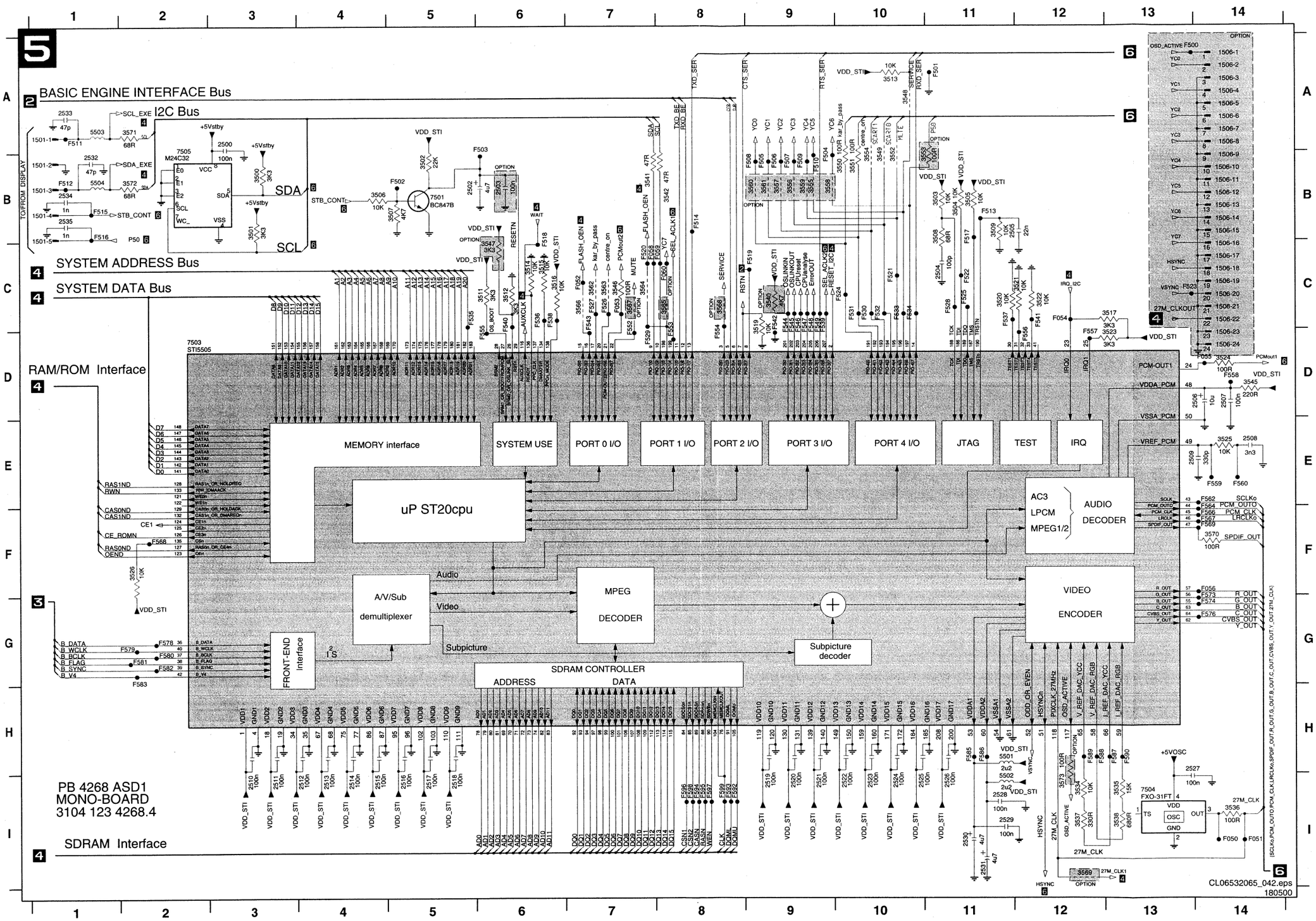
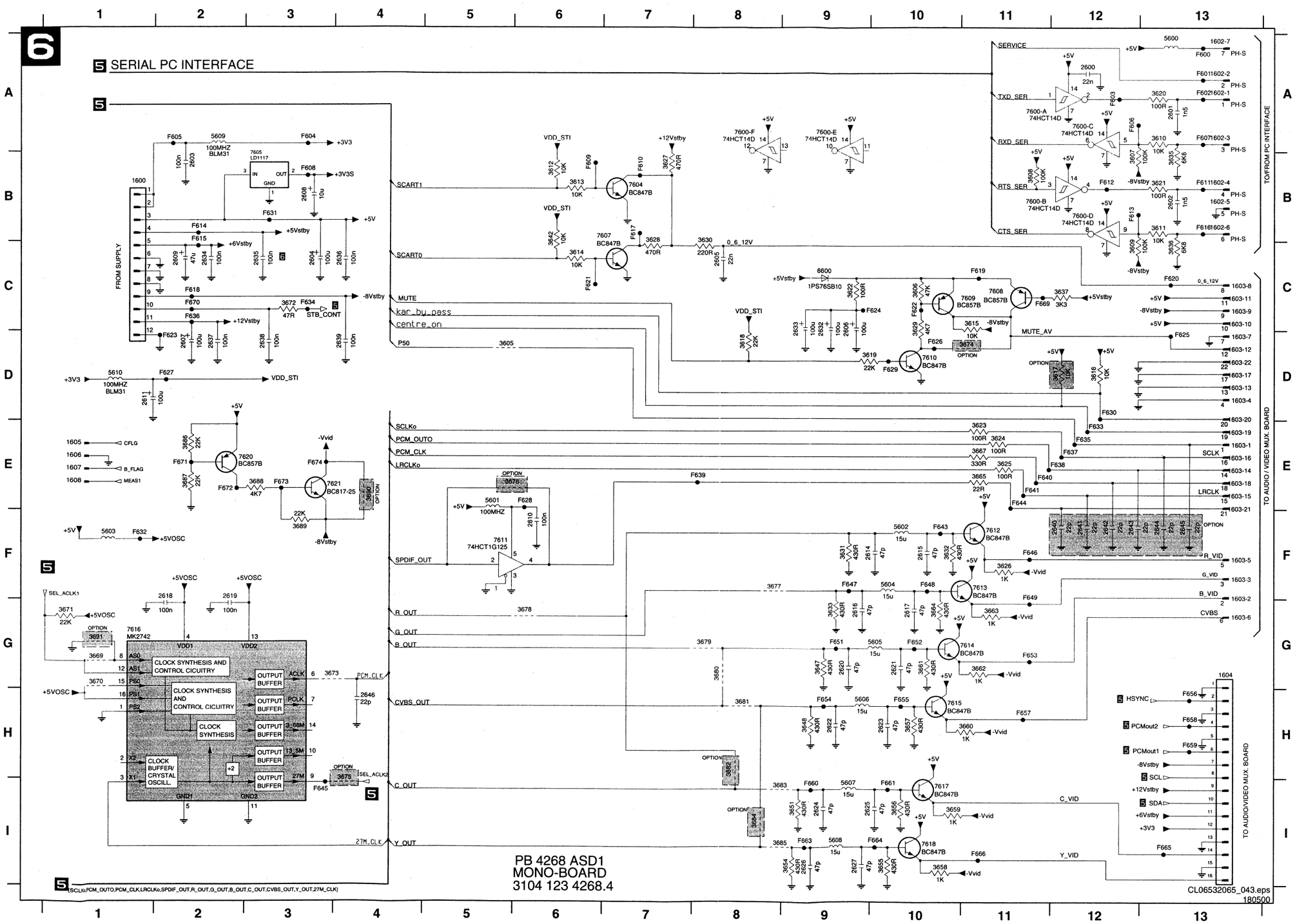
STI 5505



1501-1 A1	3565 C8
1501-2 B1	3566 C7
1501-3 B1	3567 C7
1501-4 B1	3568 C8
1501-5 B1	3569 I12
1506-1 A14	3570 F14
1506-10 B14	3571 A2
1506-11 B14	3572 B2
1506-12 B14	3573 I12
1506-13 B14	5501 H11
1506-14 B14	5502 I11
1506-15 B14	5503 A1
1506-16 C14	5504 B1
1506-17 C14	7501 B5
1506-18 C14	7503 D2
1506-19 C14	7504 I13
1506-2 A14	7505 A2
1506-20 C14	F050 I14
1506-21 C14	F051 I14
1506-22 C14	F052 C7
1506-23 D14	F053 C7
1506-24 D14	F054 C12
1506-3 A14	F055 D14
1506-4 A14	F056 F14
1506-5 A14	F058 C7
1506-6 A14	F059 C8
1506-7 A14	F060 C8
1506-8 A14	F500 A13
1506-9 B14	F501 A11
2500 A3	F502 B5
2502 B5	F503 A6
2503 B6	F504 B9
2504 C11	F505 B9
2505 B11	F506 B9
2506 D14	F507 B9
2507 D14	F508 B9
2508 E14	F509 B9
2509 E13	F510 B9
2510 I3	F511 A1
2511 I3	F512 B1
2512 I4	F513 B11
2513 I4	F514 B8
2514 I4	F515 B1
2515 I4	F516 B1
2516 I5	F517 B11
2517 I5	F518 B6
2518 I5	F519 C9
2519 I9	F520 C7
2520 I9	F521 C10
2521 I9	F522 C11
2522 I10	F523 C13
2523 I10	F524 C10
2524 I10	F525 C11
2525 I10	F526 C7
2526 I11	F527 C7
2527 H13	F528 C11
2528 I11	F529 D7
2529 I11	F530 C10
2530 I11	F531 C10
2531 I11	F532 C10
2532 B1	F533 C10
2533 A1	F534 C10
2534 B1	F535 C5
2535 B1	F536 C6
3500 B3	F537 C11
3501 B3	F538 C6
3502 B5	F539 C6
3503 B11	F540 C6
3504 B11	F541 C12
3505 B11	F542 C9
3506 B4	F543 C7
3507 B5	F544 C9
3508 B11	F545 C9
3509 B11	F546 C9
3511 C6	F547 C9
3512 C6	F548 C9
3513 A10	F549 C9
3514 C6	F552 C7
3515 C6	F553 C8
3516 C6	F554 D8
3517 C13	F555 D6
3519 C9	F556 D12
3520 C11	F557 D12
3521 C12	F558 D14
3522 C12	F559 E14
3523 D13	F560 E14
3524 D14	F562 E14
3525 E14	F564 F14
3526 F2	F566 F14
3534 I12	F567 F14
3535 I13	F568 F2
3536 I14	F569 F14
3537 I12	F573 G14
3538 I13	F574 G14
3540 C9	F576 G14
3541 B7	F578 G2
3542 B8	F579 G2
3545 D14	F580 G2
3546 C7	F581 G2
3547 B6	F582 G2
3548 A10	F583 G2
3549 B10	F585 H11
3550 B10	F586 H11
3551 B10	F587 H13
3552 B10	F588 H12
3553 B11	F589 H12
3554 B10	F590 H13
3555 B9	F592 I8
3556 B9	F593 I8
3557 B9	F594 I8
3558 B9	F595 I8
3559 B9	F596 I8
3560 B9	F597 I8
3561 B9	F598 I8
3562 C7	F599 I8
3563 C7	
3564 C7	

Service interface and Back-end



1600 B1	3658 I10	F652 G10
1602-1 A13	3659 I10	F653 G11
1602-2 A13	3660 H11	F654 H9
1602-3 A13	3661 G10	F655 H10
1602-4 B13	3662 G11	F656 H13
1602-5 B13	3663 G11	F657 H11
1602-6 B13	3664 G10	F658 H13
1602-7 A13	3665 E11	F659 H13
1603-1 E13	3667 E11	F660 I9
1603-10 C13	3669 G1	F661 I10
1603-11 C13	3670 G1	F663 I9
1603-12 D13	3671 G1	F664 I10
1603-13 D13	3672 C3	F665 I13
1603-14 E13	3673 G3	F666 I11
1603-15 E13	3674 D11	F669 C11
1603-16 E13	3675 I4	F670 C2
1603-17 D13	3676 E5	F671 E2
1603-18 E13	3677 F8	F672 E2
1603-19 E13	3678 G6	F673 E3
1603-2 G13	3679 G8	F674 E3
1603-20 E13	3680 G8	
1603-21 F13	3681 H8	
1603-22 D13	3682 H8	
1603-3 F13	3683 I8	
1603-4 D13	3684 I8	
1603-5 F13	3685 I8	
1603-6 G13	3686 E2	
1603-7 D13	3687 E2	
1603-8 C13	3688 E3	
1603-9 C13	3689 F3	
1604 G13	3690 E4	
1605 E1	3691 G1	
1606 E1	5600 A13	
1607 E1	5601 E5	
1608 E1	5602 F10	
2600 A12	5603 F1	
2601 A13	5604 F10	
2602 B13	5605 G10	
2603 B2	5606 H9	
2604 C3	5607 I9	
2605 C8	5608 I9	
2606 C9	5609 A2	
2607 D2	5610 D1	
2608 B3	6600 C9	
2609 C2	7600-A A11	
2610 F6	7600-B B11	
2611 D1	7600-C A12	
2614 F9	7600-D B12	
2615 F10	7600-E A9	
2616 G9	7600-F A8	
2617 G10	7604 B7	
2618 F2	7605 B3	
2619 F2	7607 B6	
2620 G9	7608 C11	
2621 G10	7609 C10	
2622 H9	7610 D10	
2623 H10	7611 F5	
2624 I9	7612 F11	
2625 I9	7613 F11	
2626 I9	7614 G10	
2627 I9	7615 H10	
2632 C9	7616 G1	
2633 C9	7617 I10	
2634 C2	7618 I10	
2635 C3	7620 E2	
2636 C4	7621 E3	
2637 D2	F600 A13	
2638 D3	F601 A13	
2639 D4	F602 A13	
2640 F12	F603 A12	
2641 F12	F604 A3	
2642 F12	F605 A2	
2643 F12	F606 A12	
2644 F13	F607 A13	
2645 F13	F608 B3	
2646 H4	F609 B6	
3505 D5	F610 B7	
3606 C10	F611 B13	
3607 B12	F612 B12	
3608 B11	F613 B12	
3609 C12	F614 B2	
3610 A13	F615 B2	
3611 B13	F616 B13	
3612 B6	F617 B7	
3613 B6	F618 C2	
3614 C6	F619 C11	
3615 C11	F620 C13	
3616 D12	F621 C6	
3617 D12	F622 C10	
3618 D8	F623 D2	
3619 D9	F624 C10	
3620 A13	F625 D13	
3621 B13	F626 D10	
3622 C9	F627 D2	
3623 E11	F628 E6	
3624 E11	F629 D10	
3625 E11	F630 D12	
3626 F11	F631 B3	
3627 B7	F632 F1	
3628 C7	F633 E12	
3629 C10	F634 C3	
3630 C8	F635 E12	
3631 F9	F636 C2	
3632 F10	F637 E12	
3633 G9	F638 E12	
3635 B13	F639 E8	
3636 C13	F640 E11	
3637 C12	F641 E11	
3642 B6	F643 F10	
3647 G9	F644 E11	
3648 H9	F645 I3	
3651 I9	F646 F11	
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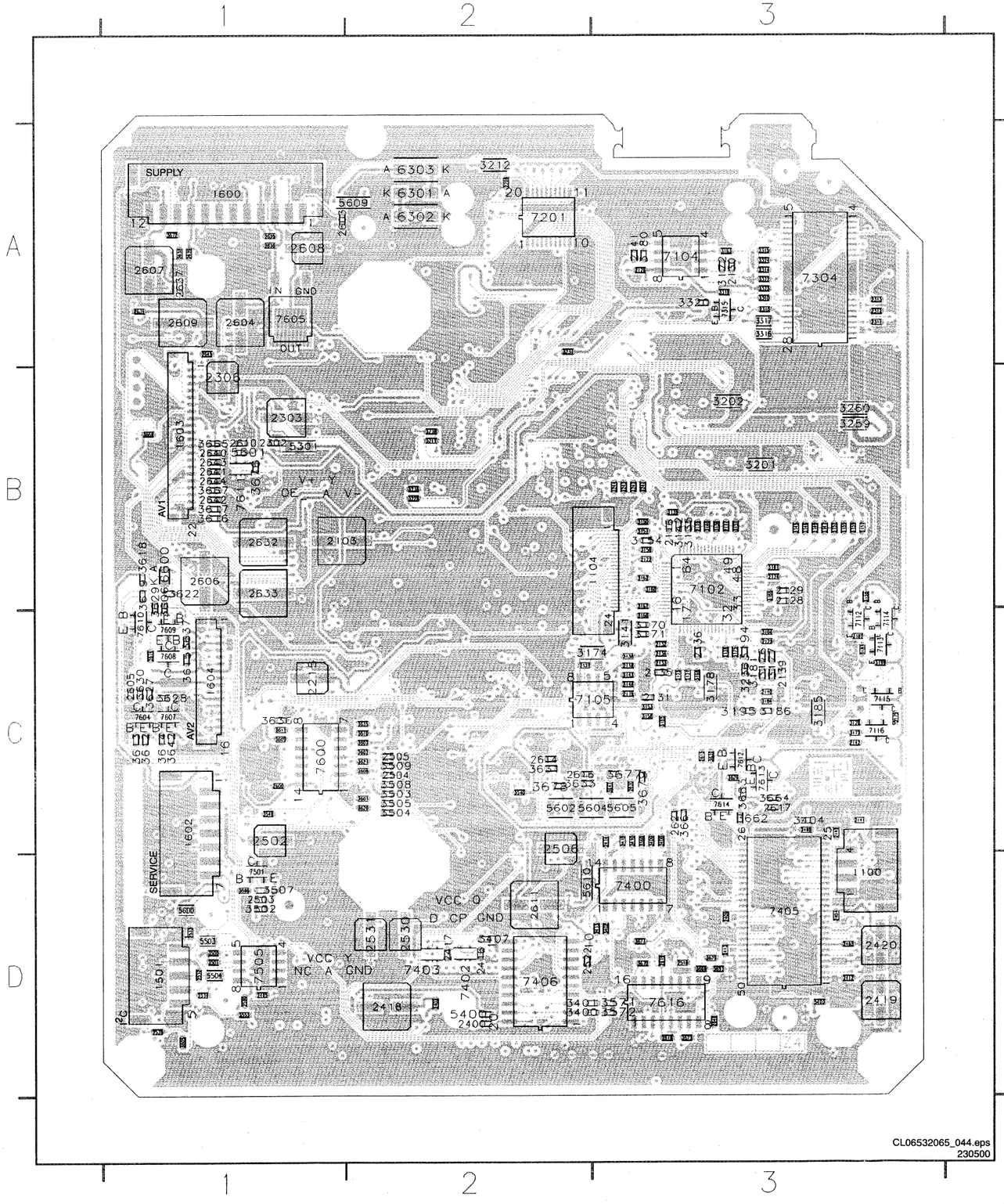
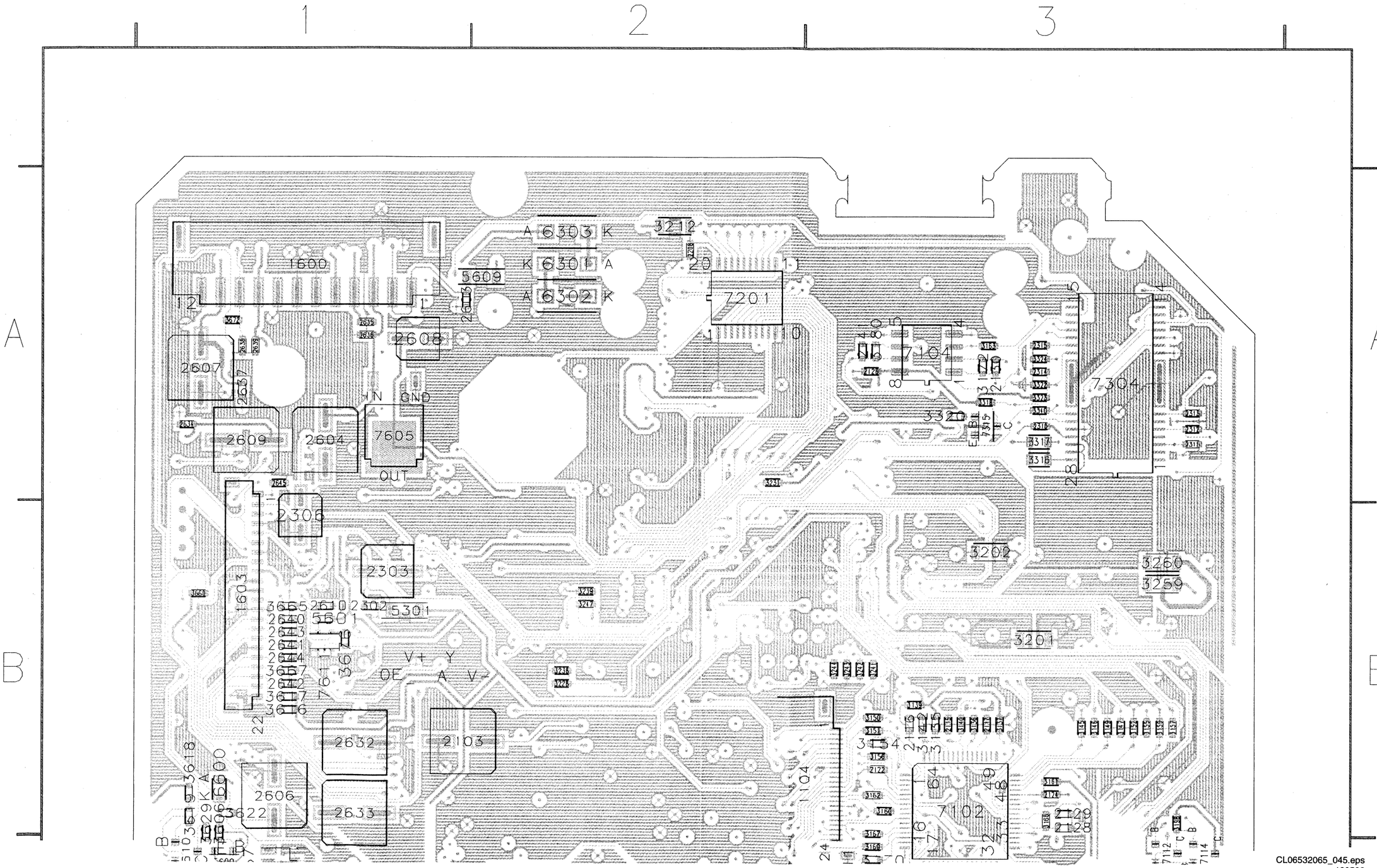
3657 H10	F651 G9	

Top view



1100	D3	2618	D3	3318	A3	5609	A2
1104	B3	2619	D3	3320	A3	5610	D2
1501	D1	2620	C3	3322	A3	6301	A2
1600	A1	2621	C3	3323	A3	6302	A2
1602	C1	2632	B1	3324	A3	6303	A2
1603	B1	2633	B1	3340	A3	6600	B1
1604	C1	2634	A1	3400	D2	7102	B3
2103	B1	2635	A1	3401	D2	7104	A3
2115	B3	2636	A1	3402	D3	7105	C3
2116	B3	2637	A1	3404	C3	7112	C3
2117	B3	2638	A1	3406	C3	7113	C3
2118	C3	2639	A1	3407	D2	7114	C3
2119	C3	2640	B1	3409	C3	7115	C3
2122	B3	2641	B1	3410	C3	7116	C3
2123	C3	2642	B1	3418	C3	7201	A2
2124	B3	2643	B1	3500	D1	7304	A3
2125	C3	2644	B1	3501	D1	7315	A3
2126	A3	2645	A1	3502	D1	7400	D3
2127	C3	2646	D3	3503	C2	7402	D2
2128	B3	3120	C3	3504	C2	7403	D2
2129	B3	3135	B3	3505	C2	7405	D3
2130	A3	3136	B3	3506	D1	7406	D2
2131	C3	3137	B3	3507	D1	7501	D1
2132	C3	3138	C3	3508	C2	7505	D1
2133	C3	3139	B3	3509	C2	7600	C1
2134	C3	3140	B3	3540	C2	7604	C1
2135	C3	3141	C3	3548	C1	7605	A1
2136	C3	3142	B3	3553	D1	7607	C1
2137	C2	3143	C3	3569	C3	7608	C1
2138	C3	3145	B3	3571	D3	7609	C1
2139	C3	3146	B3	3572	D3	7610	C1
2140	C3	3147	B3	3605	D1	7611	B1
2141	A3	3148	C3	3606	B1	7612	C3
2142	C3	3149	B3	3607	C2	7613	C3
2144	C3	3150	B3	3608	C2	7614	C3
2145	C3	3151	B3	3609	C1	7616	D3
2208	A2	3152	B3	3610	C2		
2215	C1	3153	C3	3611	C1		
2302	B1	3154	B3	3612	C1		
2303	B1	3155	B3	3613	C1		
2306	B1	3156	B3	3614	C1		
2310	A3	3157	B3	3615	C1		
2311	A3	3158	C3	3616	B1		
2312	A3	3159	B3	3617	B1		
2313	A3	3160	B3	3618	B1		
2314	A3	3161	B3	3619	B1		
2315	A3	3162	B3	3620	C2		
2400	D2	3163	A3	3621	C2		
2403	D3	3164	C3	3622	B1		
2404	D3	3165	C3	3626	C3		
2405	D1	3166	B3	3627	C1		
2408	C3	3167	B3	3628	C1		
2409	D3	3168	C3	3629	B1		
2412	D3	3169	C3	3630	C1		
2413	D3	3170	C3	3631	C2		
2414	C3	3171	C3	3632	C3		
2415	D3	3172	A3	3633	C2		
2416	D2	3173	C3	3635	C2		
2417	D2	3174	C3	3636	C1		
2418	D2	3175	C3	3637	C1		
2419	D3	3176	C3	3642	C1		
2420	D3	3177	C3	3647	C3		
2500	D1	3178	C3	3660	B1		
2502	C1	3179	C3	3661	C3		
2503	D1	3180	A3	3662	C3		
2504	C2	3181	C3	3663	C3		
2505	C2	3182	C3	3664	C3		
2506	C2	3183	C3	3665	B1		
2518	D3	3184	C3	3667	B1		
2522	D2	3185	C3	3669	D3		
2530	D2	3186	C3	3670	D3		
2531	D2	3194	C3	3671	D3		
2532	D1	3195	C3	3672	A1		
2533	D1	3198	B3	3673	D3		
2534	D1	3199	C3	3674	C1		
2535	D1	3201	B3	3675	D3		
2600	C1	3202	B3	3676	B1		
2601	C2	3212	A2	3677	C3		
2602	C2	3228	B2	3678	C2		
2603	A1	3231	A2	3679	C3		
2604	A1	3236	C3	3691	D3		
2605	C1	3238	B2	5301	B1		
2606	B1	3239	B2	5400	D2		
2607	A1	3241	B3	5402	D2		
2608	A1	3242	B3	5403	D3		
2609	A1	3243	B3	5503	D1		
2610	B1	3244	B3	5504	D1		
2611	D2	3247	B2	5600	D1		
2614	C2	3259	B3	5601	B1		
2615	C3	3260	B3	5602	C2		
2616	C2	3316	A3	5604	C3		
2617	C3	3317	A3	5605	C3		

Detailed Top view 1



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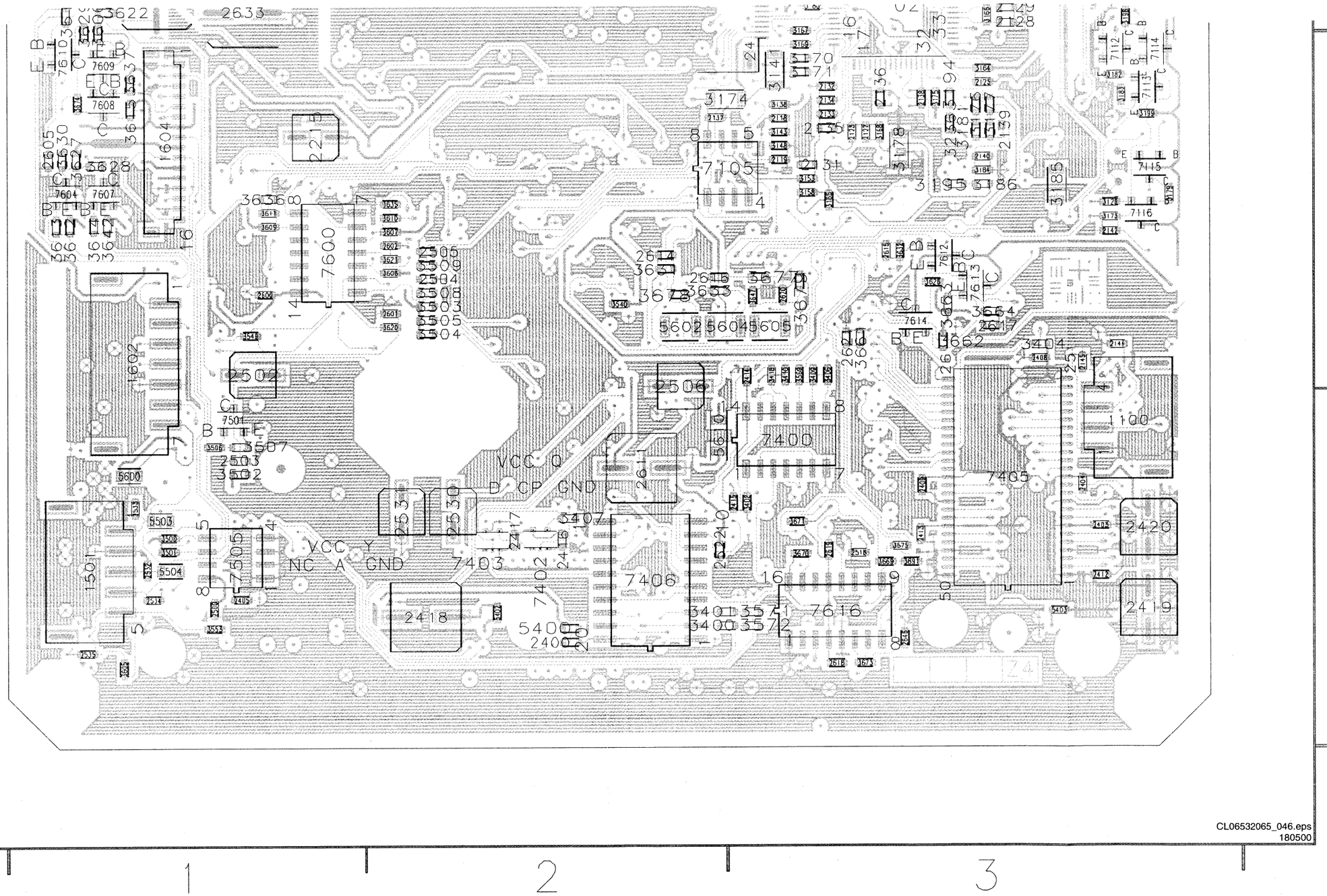
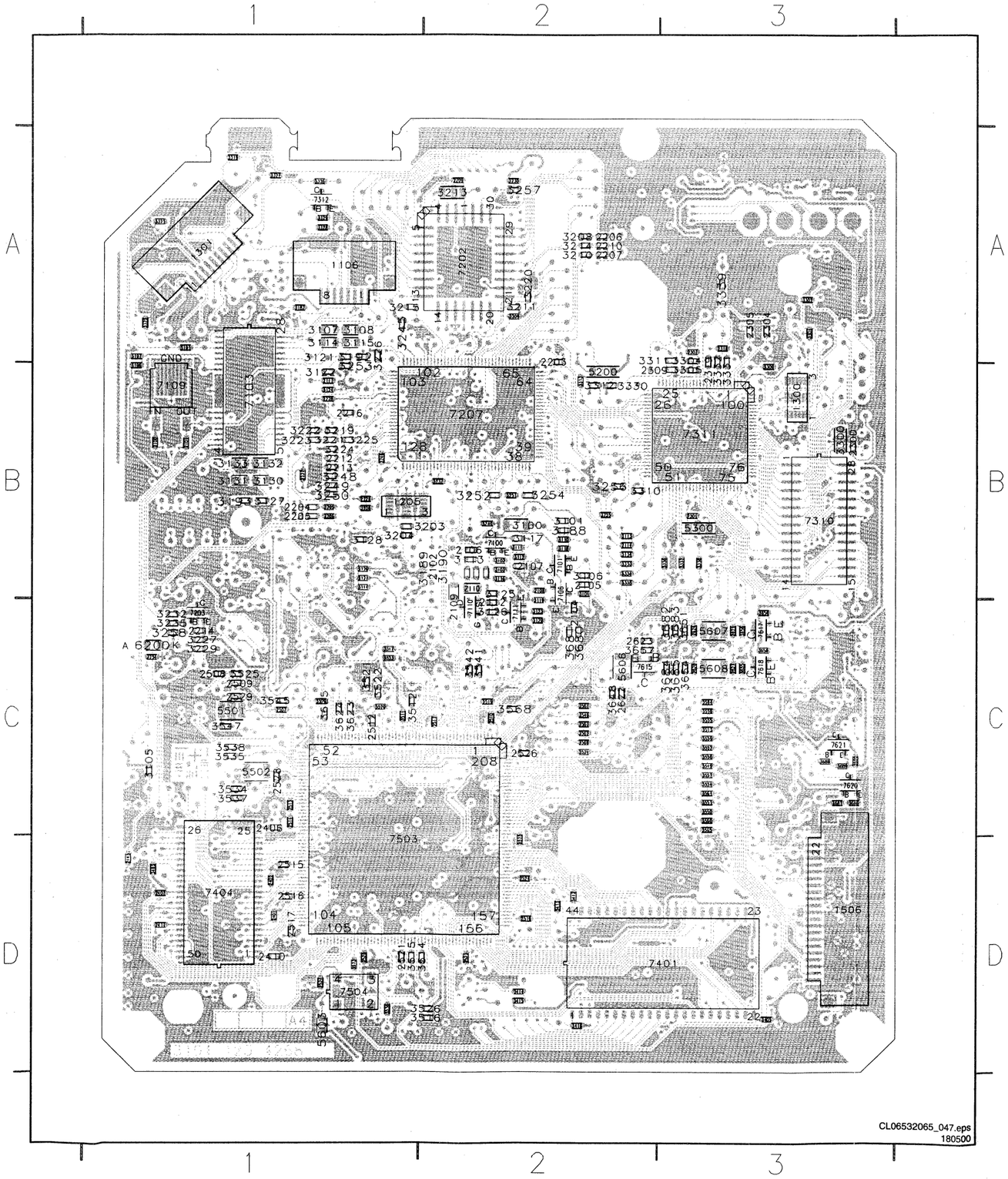
Detailed Top view 2



Bottom view



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1300	B3	3119	C2	3403	D1	7207	B2
1301	A1	3121	A1	3405	D3	7310	B3
1506	D3	3122	B1	3412	D2	7311	B3
2100	B1	3123	C2	3413	D2	7312	A1
2101	B1	3124	B1	3414	D2	7401	D3
2102	B2	3125	B2	3415	D2	7404	D1
2104	C2	3126	C2	3416	D2	7503	D1
2105	B2	3127	B1	3511	C1	7504	D1
2106	B2	3128	B1	3512	C1	7615	C2
2107	B2	3129	C2	3513	C3	7617	C3
2108	B2	3130	B1	3514	D2	7618	C3
2109	C2	3131	B1	3515	D1	7620	C3
2110	B2	3132	B1	3516	D2	7621	C3
2111	B1	3133	B1	3517	C1		
2112	C2	3134	B2	3519	C2		
2113	B2	3144	B1	3520	C1		
2114	B2	3187	A1	3521	C1		
2120	B1	3188	B2	3522	C1		
2121	B1	3189	B2	3523	C1		
2143	D1	3190	B2	3524	C2		
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2205	B1	3193	B1	3534	C1		
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2207	A2	3197	A1	3536	D1		
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2216	B1	3208	A2	3546	C2		
2226	B1	3209	A2	3547	C1		
2227	B1	3210	A2	3549	C3		
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2309	B2	3221	B1	3557	C3		
2318	A3	3222	B1	3558	C3		
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2508	C1	3234	C1	3567	C2		
2509	C1	3235	C1	3568	C2		
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2514	C1	3248	B1	3625	C1		
2515	D1	3249	B1	3648	C2		
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2517	D1	3251	B2	3654	C3		
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2521	D1	3254	B2	3657	C3		
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2525	D2	3257	A2	3680	C2		
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2528	C1	3301	A3	3683	C3		
2529	C1	3302	A3	3684	C3		
2622	C2	3304	A3	3685	C3		
2623	C2	3305	B3	3686	C3		
2624	C3	3309	B3	3687	C3		
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2627	C3	3312	B2	3690	C3		
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3112	B2	3333	B2	7103	B1		
3113	B2	3334	B2	7106	B2		
3114	A1	3335	B2	7109	B1		
3115	A1	3336	B3	7110	C2		
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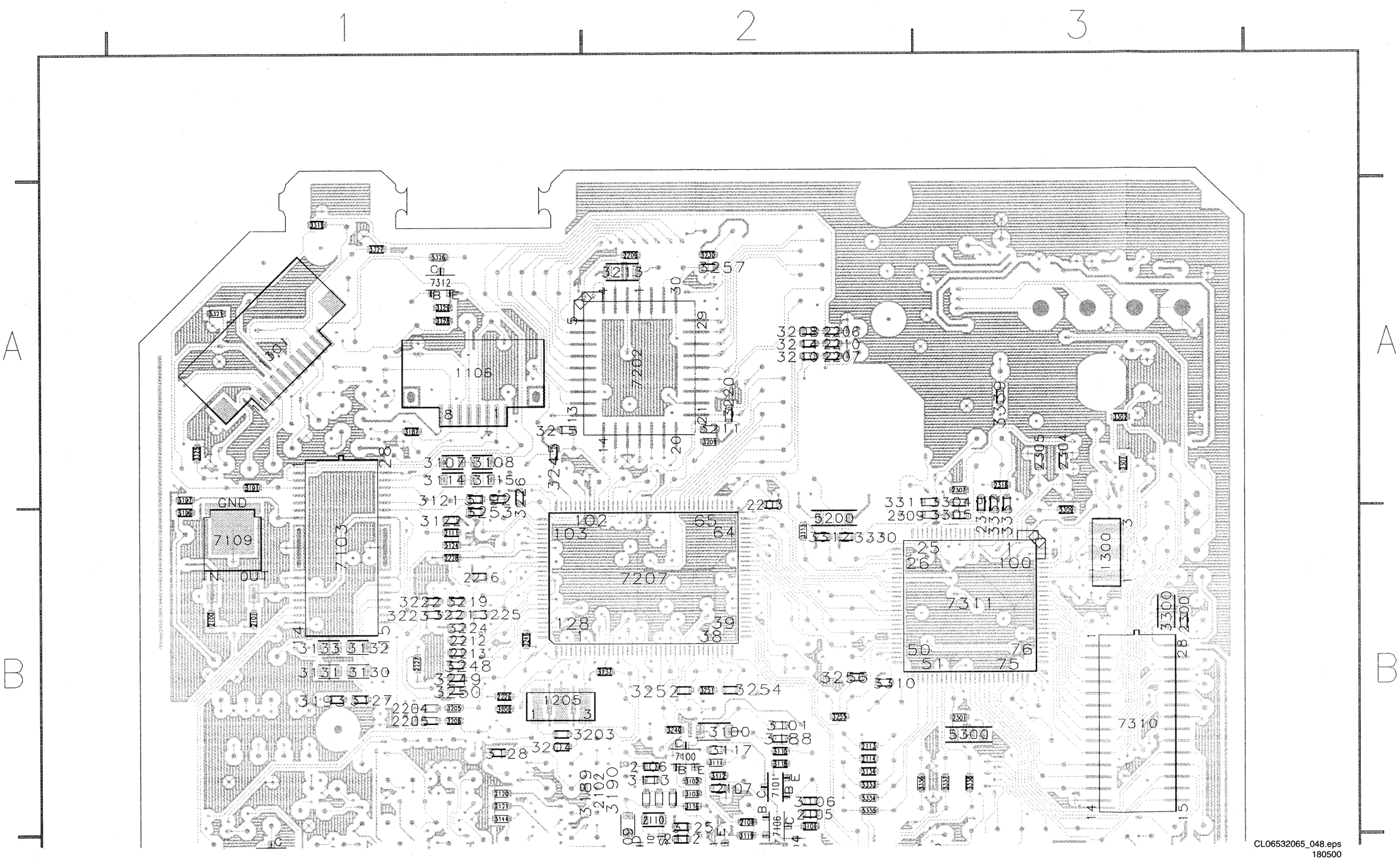
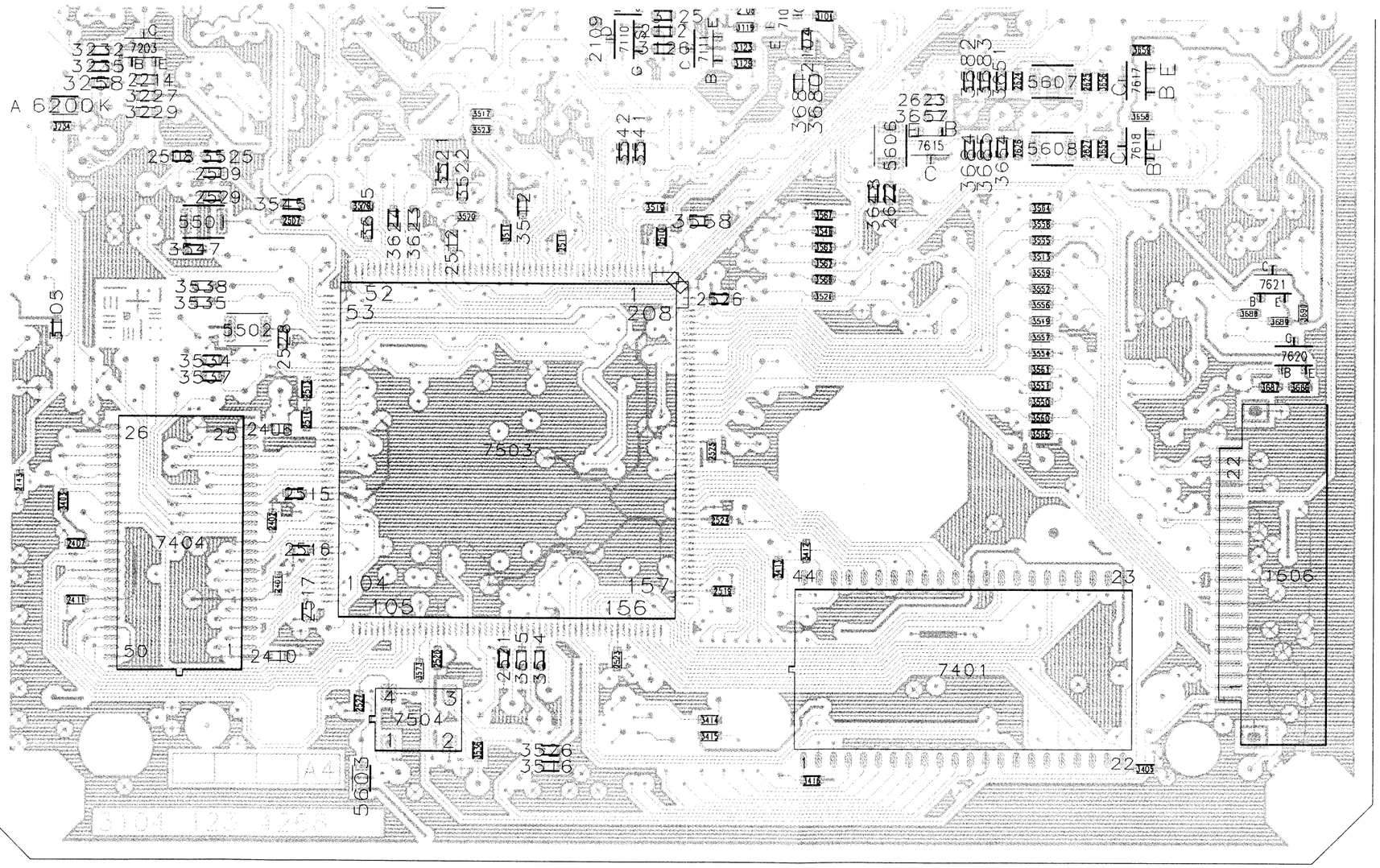
Detailed Bottom view 1



Detailed Bottom view 2



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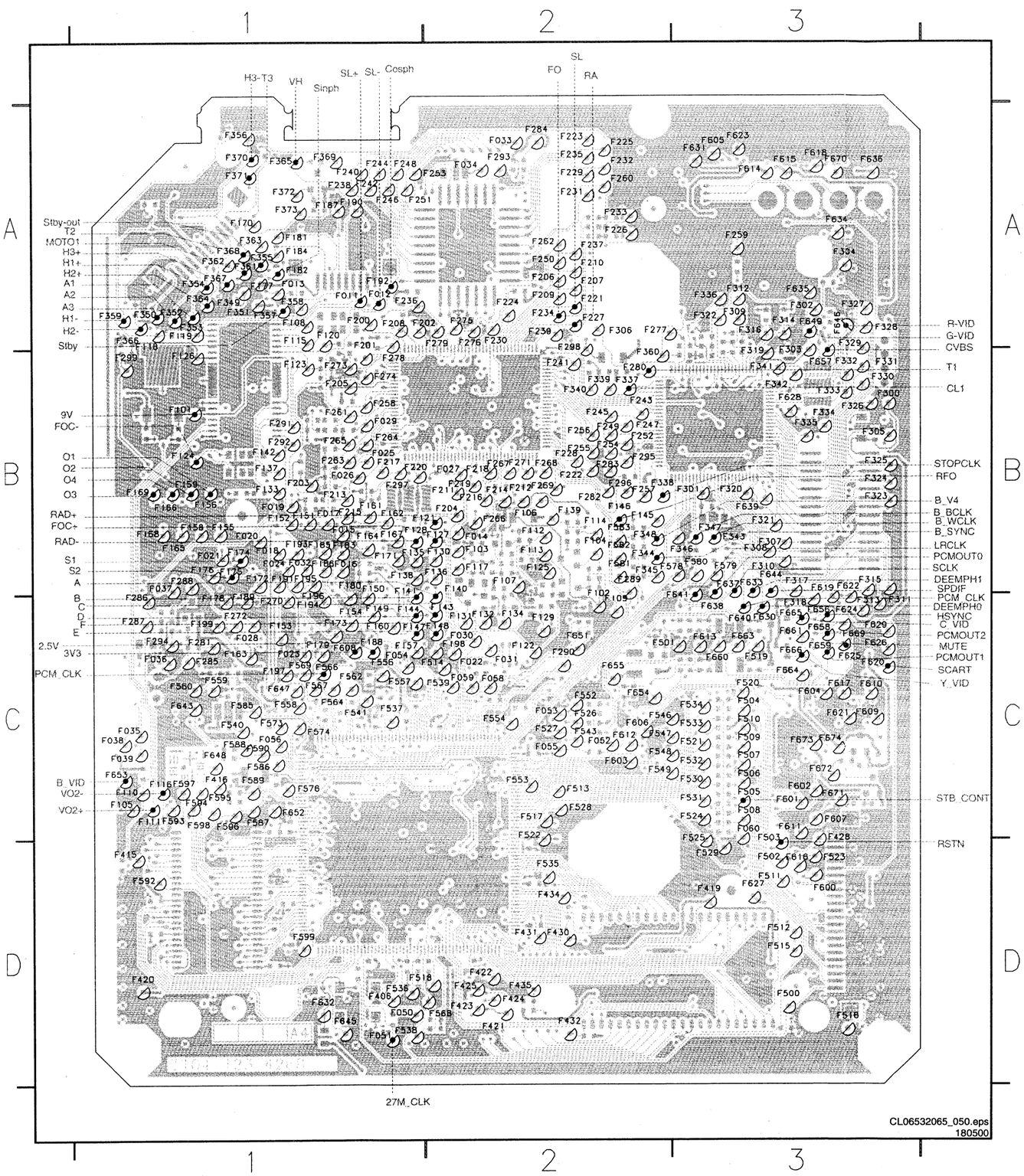
180500

Testpoint overview



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F014	B2	F154	C1	F243	B2	F332	B3	F531	C3	F636	A3
F015	B1	F155	B1	F244	A1	F333	B3	F532	C3	F637	B3
F016	B1	F156	B1	F245	B2	F334	B3	F533	C3	F638	C3
F017	B1	F157	C1	F246	A1	F335	B3	F534	C3	F639	B3
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F021	B1	F161	B1	F250	A2	F339	B2	F538	D1	F644	B3
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F039	C1	F179	C1	F268	B2	F357	A1	F561	C1	F663	C3
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F106	B2	F195	B1	F284	A2	F373	A1	F577	B3		
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F143	C2	F232	A2	F321	B3	F520	C3	F625	C3		
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F145	B2	F234	A2	F323	B3	F522	C2	F627	C3		
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F148	C2	F237	A2	F326	B3	F525	C3	F630	C3		
F149	C1	F238	A1	F327	A3	F526	C2	F631	A3		
F150	B1	F239	A2	F328	A3	F527	C2	F632	D1		

Personal notes:

Personal notes:

8. Alignments

No alignments available

9. IC Descriptions.

9.1 SAA7399 (MACE2) General.

Mace2 is a name used for the successor of the ACE1 IC. The term MACE (mini-ACE) is used because MACE2 does not have a decoder on board. Application area's: Mainly CD-R(W) and prototyping of DVD(-ROM) or high speed CD-ROM.
Functions implemented on-board of MACE2:
A further improved digital servo module. Derived from the ACE1 servo module, but with improvements (make the input switchable between diode signal and error signal processing, improved brake).
The 80C51 micro-controller with external ROM.
The OPC. Optimum Power calibration, used for CDR.
The PCS. Position Control Sledge. A way to speed up sledge movement using hall sensors.

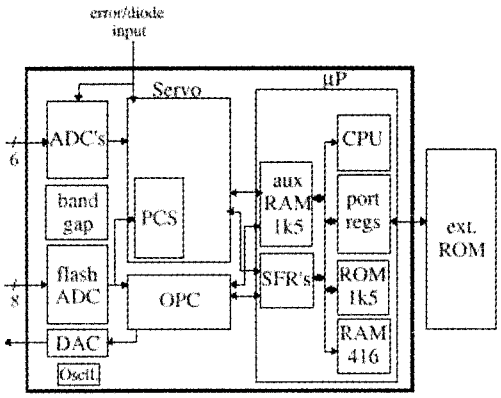


Figure 9-1 Overall block diagram MACE2.

9.2 Features

- Focus and Radial servo loop.
- Built-in access procedure.
- Selectable servo error or servo diode inputs.
- Focus noise performance equivalent to DSICS
- Automatic closed loop gain control available for focus and radial loops
- High speed track crossing velocity measurement > 350 kHz.
- Fast Radial Brake circuitry.
- Sledge motor servo loop, with pulsed sledge support and PCS
- Incorporated micro-controller equivalent to 80C51 --> 66MHz.
- Programmable wait state controller.
- Two embedded RAM's of 416 bytes and 1.5 kB res.
- Optimum Power Calibration Hardware support up to write at N=8.
- Debug facilities.
- Memory mapped interface to sub-modules.
- Programmable clock multiplier.
- 8 Multipurpose I/O lines.
- 5 external interrupt lines.
- External Flash ROM support.
- Sledge stepper motor support.

9.3 The Digital Servo block.

In a CD system, there are some 12 control loops active. About six of them are needed to adjust the servo error signals, that is once per disc rotation offsets, signal amplitudes and loop gains (AGC's) are adjusted to enlarge system robustness and to avoid expensive potentiometer adjustments in production. The other six loops determine the laser spot position on the disc in the radial, axial (focus) and tangential directions. The servo in MACE2 takes care of these controls.
The servo inside Mace2 also has to take care that the spot accesses a required position as fast as possible. This access system consists of two parts, namely the actuator and the sled, which are within a certain range, mechanically and electrically independent. So during an access the servo has to control as well the actuator as the sled.

9.4 Functional description servo

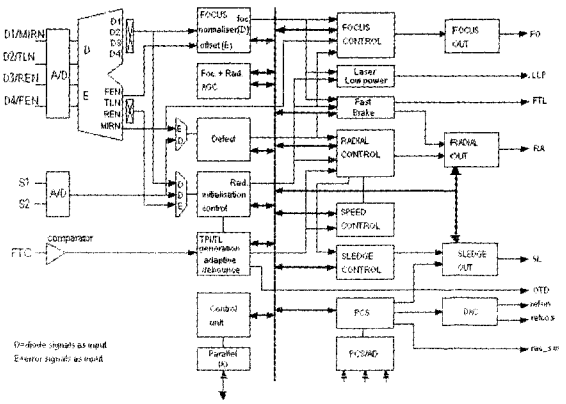


Figure 9-2 Mace2 servo block diagram.

The following functions can be distinguished:
- A to D conversion: a direct AD-conversion of the diode/ error currents.
- Pulse density D to A conversion: Noise shaper output stages.
- Control unit: Provides mainly the communication and on/ off functions.
- Focus normaliser: A partial division of focus and sum signal. Special saturating provisions are included when dividing through very small numbers.
- Initialisation control: Includes the radial normaliser, automatic radial offset compensation and level initialisation for the Track Position Indicator(TPI) for both diode and error input signals.
- TPI/TL generation and adaptive debounce: Generates Track loss (TL) which is protected against disc defects. The TL is made out of the unprotected TPI signal. The debouncer (with improved debounce times) minimises the disturbing effect of HF on the TL and RF crossovers for the track count circuitry.

- Defect detector: Holds the focus and/or radial control signal on disc dropouts.
- Speed control: Used during access. With radial actuator feed forward.
- Focus control: PID controller with wide range adjustable characteristics.
- Radial control: PID controller with wide range adjustable characteristics.
- Sledge control: PID controller with wide range adjustable characteristics and a pulsed sledge controller.
- Laser Low Power: Switches the laser from write back to read power whenever the device tends to go off-track.

9.5 Input circuits servo

Five out of six of the MACE2 servo inputs can be switched between diode current inputs (for audio and data application) and error signal inputs (for recordable applications).
The analogue signals from the diode pre processor are converted into a digital representation using A/D converters.

9.6 Focus control.

9.6.1 Focus start-up.

To bring the actuator in focus position a triangular shaped voltage is applied to the actuator to perform a search movement. When the lens moves from or to the disc, CA (central aperture) is monitored to reach a certain programmable absolute level. When this value is CA level is reached, the FOK signal becomes true and FEn is passed to the FEn level detector.
At the moment this FEn level is reached the wait for the focus mode is entered and the focus control loop is enabled to detect a sign inversion in the FEn signal.
When this zero crossing in this FEn signal is detected, the loop is closed to function as PID controlled loop and is switched to the PID mode.
During focus start-up a dither signal is added to the output signal of the integrator. It prevents the actuator from hitting its natural resonance. With this technique quantisation, effects are compensated for during start-up.

9.6.2 Focus Position Control loop.

The focus control loop contains a digital PID controller that has 5 parameters available to the user. These coefficients influence the integrating, proportional and differential action of this PID and a digital low pass filter following the PID. The fifth coefficient influences the loop gain.

9.6.3 Dropout detection.

This detector can be influenced by one parameter. The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false, it is assumed as caused by a black dot in the first place.

9.6.4 Focus Loss detection and Fast restart.

Whenever FOK is false longer than about 2 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the uP-programmed coefficients.

9.6.5 Focus Automatic Gain Control loop.

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop that is used to correct the loop gain. Since this decreases the optimal performance, the gain control should only activated shortly (for instance when starting a new disc).

9.7 Radial control.

The MACE2 digital controller includes the following radial servo functions:

9.7.1 Level initialisation:

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain, offset and satellite sum/MIRN signal gain for TPI level generation. The initialisation procedure runs in a radial open loop situation and is < 200 ms. This start-up time period may coincide with the last part of the turntable motor start-up time period.

9.7.2 Automatic gain adjustment:

Because of this initialisation the amplitude of the RE signal is adjusted within _10% around the nominal RE amplitude.
Offset adjustment: The additional offset in RE due to the limited accuracy of the start-up procedure is less than +/- 50nm.

9.7.3 TPI level generation:

The accuracy of the initialisation procedure is such that the duty cycle range of TPI becomes 0.4 < duty cycle < 0.6.

Sledge home:
Sledge moves to reference position at the inner side of the disc with user defined voltage.

Tracking control:
The actuator is controlled using a PID loop filter with user defined coefficients.

Access:
In Mace2 there are two fundamentally different ways to perform an access:

Using the PCS
A more detailed description of this access method is given in an other section.

Using the servo controlled access:
The way it was done in the predecessors of Mace2.This access procedure is divided into 3 different modes, depending on the requested jump size:
access type size access speed
Actuator jump decreasing velocity
Sledge jump maximum power to sledge 1
Controlled sl. jump controlled brake power
The access procedure makes use of a track counting mechanism, a velocity signal based upon the number of tracks passed within a fixed time interval, a velocity setpoint calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.
If the number of tracks to jump is too large, then the Sledge jump mode is activated, else the actuator jump is performed.
The requested jump size together with the required sledge braking distance at maximum access speed defines the value of the maximum numbers of tracks.
During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the integrator contents of the actuator. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction, while the actuator becomes idle.

Radial Automatic Gain Control loop:
The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimal performance the gain control should only be activated shortly (for instance when starting a new disc). This gain control differs from the earlier mentioned level initialisation. This level initialisation should be done first. The level initialisation without the gain control reduces tolerances from the front-end only.

9.8 The radial PID.

Since we are dealing with a big variety of applications and drives, the servo controllers in MACE2 should be adjustable within a large frequency range.
In order to read out the track properly -a track consists of sequential ordered data pit's which hold audio, video or ROM data - the focus and radial position controls must follow the moving track within some tenths of a micrometer, despite of disc imperfections and external disturbances.
For instance, a rotating disc causes, due to track eccentricity, track unroundness, or disc skew, track movements up to some millimetres. The control loop reduces this to about one tenth of a micrometer.

9.9 Initialisation control.

Due to optical, electrical and mechanical tolerances in CD players, properties of the servo signals such as offset and gain can vary. In general, without proper signal processing, a simple PID controller function cannot cope with this relatively large offset and gain spreads. Therefore, gain and offset adjustments during manufacture or active control, to compensate for these signal imperfections, become inevitable.
Adjustment procedures in the factory are expensive. So, automatic adjustment procedures have been implemented in order to avoid most of the potentiometer adjustments. In the MACE2 servo automatic adjustments are applied to the radial error signal only.

9.10 The AGC.

The Automatic Gain Control is used in the MACE2 digital servo to adjust the radial and focus bandwidths to a nominal value. Injecting a signal in the loop and measuring the phase of its resulting signal (wobble method) does this.
Principle of the Automatic Gain Control.
The principle of the Automatic Gain Control (AGC) circuit, as used in MACE2, is drawn in the next figure.

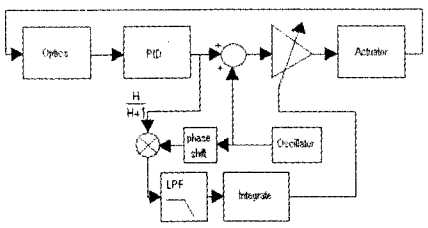


Figure 9-3 Principle of the automatic gain control.

A sine wave signal with a certain frequency is injected in the control loop at the summation point. The resulting signal is measured before the injection point. The injected signal is shaped by H/1+H . This measured signal is multiplied by a phase shifted version of the injected signal. The result of the multiplication is low pass filtered and integrated. (The integrator is started at the nominal gain of the control loop). The result of the integration is fed to the adjustable loop gain. This principle, synchronous detection, is also known as 'wobble method'.

9.11 The Fast brake.

The fast brake is an aid to speed up radial capture after a high-speed jump. It is a separate radial control with a much higher bandwidth. The radial control output can be switched between fast brake mode and original radial control mode. The fast brake helps the radial actuator at the end of a jump to "stick" to the right track. In fast brake mode, the actuator starts to follow the track movements. It's a bit like jumping on a moving train. If you run as fast as the train, you can just step in. After a radial open loop jump the tracks are moving (as a result of eccentricity) at a very high speed underneath the radial actuator. This speed is too high for a normal radial control loop to do radial capture. When the radial control is switched over to fast brake mode for a short term, this moving of the tracks underneath the actuator becomes much slower, (because the actuator follows the track movement), so when you switch back to original radial control, it's much easier to do radial capture.

9.12 The Defect Detector.

Because of the possible earlier mentioned defects (fingerprints, etc) a defect detection circuit is incorporated into the MACE2 servo. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability.

9.12.1 Operation:

The defect detector prevents the light spot from going out of focus and going off track due to disc dropout excitations. The defect detector can be switched on and off under software control and can be applied to the focus control only, or both to the focus and radial control.
Whenever this circuit detects a defect, it will hold all radial and focus controls.
The hold signal is generated whenever the reflected light intensity drops rapidly (< 1:5 ms) down to roughly 75% of the actual intensity level. In that case the output of the comparator becomes active and controls the focus and radial signal switch.
This circuit improves the playability of the application (black dot performance, etc) and is programmable to optimise it for specific disc defects. The actions of this circuit can be monitored on the DEFO pin (active high).
An external defect detection circuit can be added by removing the connection between DEFO and DEFI (normal operation) and inserting the external circuitry.
These signals are afflicted with some uncertainties caused by:

- Disc defects like scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

9.13 Laser Drive On.

The LDON pin is used to switch the laser drive off and on. It is an open drain output. In case the laser is on, the output has a high impedance. The pin will be automatically driven if the focus control loop is switched on.

9.14 Laser Low Power (LLP).

The LLP output can be used by write-able systems to switch the laser back to read power when the light spot goes off-track while writing discs. To prevent that the neighbour tracks are damaged when the spot goes off-track the laser has to be switched very fast to the safe read power. The laser is not switched off (like LDON does), so the system can carry on reading.
The tracking (radial) and focus error signals are used to disable the laser write power. This is done through the LLPn, active low Laser Low Power, signal. Note that LLPn is a servo output, which is inverted before it is output via the LLP pin, so the LLP pin is active high.
So, if any of the following conditions is true, the laser write power is disabled by the MACE2 servo.

- Off Track, more than a quarter off a track away from the correct one
- ORD, radial error signal too large. Larger than the given setpoint, which should be chosen at a critical write failure level. An adjustable band pass filter first processes the radial error signal.
- OFD, focus error signal too large. Larger than the given setpoint, which should also be chosen with care. An adjustable band pass filter also first processes the focus error signal. All settings of the focus and radial part are independent.
- OTR, prot stat flag which becomes active if ORD becomes active during an actual laser write (LWR) action. This flag is reset only by a status read (RSTAT) command. So until then LLPN stays active.
- OFO, prot stat flag that becomes active if OFD becomes active during an actual laser write action. Same idea as OTR.

This error detection circuit can be switched off (apart from the Off Track detection) by raising the setpoint levels to its maximum value.

9.15 The OPC.

The OPC block in Mace2 is used for the following functions:

- During write actions, it stores Pw samples, which can be evaluated by the microprocessor.
- During OPC read actions, it stores A1, A2 and CALF samples, which are used for calculating the asymmetry and the modulation index.
- The OPC block is used for EFM detection.
- During reading of a disc, it stores A1 and CALF samples, which can be monitored.

Although the OPC block is used for multiple functions, it got it's name from the OPC procedure, which is it's main task.
The OPC (Optimum Power Calibration) procedure is used in CD-R/CD-RW/DVD-RAM applications. It is used to "calibrate" the laser write power in writable systems.
It reads in 3 analogue signals from an analogue pre-processor like AEGER-2 (A1, A2, and CALF) and the actual write power (Pw) from the laser controller and feeds an analogue output signal Alpha0 back to AEGER-2. A1, A2 and CALF represent the max, min and average value of the EFM signal respectively. Alpha0 controls the laser write power. All analogue signals are converted to an 8 bit digital signal. Conversion frequency at 16.9MHz base clock is 88kHz (each channel).

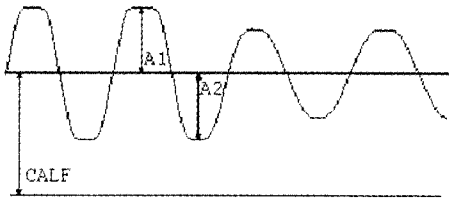


Figure 9-4 Definition of the A1, A2 and CALF signals.

9.16 Definition of terms.

The asymmetry (and modulation index m of the EFM signal are calculated from the analogue inputs:

$$\beta = \frac{A1 - A2}{A1 + A2}$$

$$m = \frac{A1 + A2}{A1 + CALF}$$

9.17 Rough description of the OPC procedure

Basically the OPC procedure tries to find out the optimum laser power to be used on a specific disc. The OPC procedure uses about 15 ATIP frames. These frames are located in the "PCA" area. This is a special part of the disc used only for power calibration. The drive first checks whether there are 15 frames "empty" in the PCA. Next the OPC is performed in these 15 frames.
The OPC operation consists of two stages: A "write" and a "read" stage. First 15 ATIP frames are written (during which the OPC block stores Pw samples), and then the same 15 ATIP frames are read back again, (during which the OPC block stores A1, A2 and CALF samples). During the write stage, random EFMis written in a test area located on the inner side of the disc. During this recording the write power is increased stepwise from a low to a high power level.

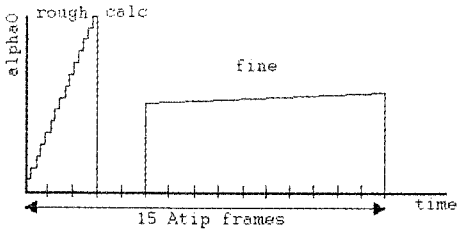


Figure 9-5 Figure 5: OPC write profile.

First during 3 ATIP frames the power is increased in rather big steps (rough OPC). During this action Pw samples are stored into memory. During the rough OPC, the OPC makes 7 steps per ATIP frame. This gives 21 samples into the OPC memory. From these samples, the microprocessor can calculate what's roughly the best alpha0 setting for this typical disc.
After 2 frames of calculations, another 10 ATIP frames are written using smaller steps (fine OPC) around the alpha0 setting, which gave the best result during the rough OPC.
The second stage of the OPC procedure is the "read" phase

in which the pattern recorded in the previous stage is read back.
During this read phase the OPC block stores A1, A2 and CALF samples from exact the same location where during the OPC write phase the Pw samples where stored. The samples for A1, A2, CALF and Pw are listed side by side into memory. After the read back phase the processor calculates at which setting of alpha0 the least jitter is encountered. This setting will be used to write the disc with.

9.18 The OPC top level.

The OPC block as a whole has 5 possible modes:
- Recording mode: This can be either OPC writing (writing EFM test patterns to disc and Alpha0 stepping) or standard write mode (i.e. alpha0 is constant).
- OPC reading: Reading back OPC test patterns from disc.
- Normal read mode: detects the presence of EFM.
- DVD read mode: used for DVD-RAM experiments.
- EFMD only mode: no data being written to the AUX RAM, but the EFM detector and the PW monitor still running. Contents of the QUX RAM remain unchanged.

All actions in the OPC hardware are synchronised to the ATIP frame sync, which can be either generated internally or received from the encoder/decoder during writing. The microprocessor writes data asynchronously to the OPC hardware. The OPC block synchronises this data to the sync either internally generated, or obtained from CDR60.

9.19 The Analogue to Digital converter.

The analogue to digital converter of the OPC is shared with the ADC required by the PCS.

9.20 The digital input filters.

The combined ADC for the OPC and the PCS delivers a multiplexed stream of 8 bit words. A sequential low-pass filter filters this multiplexed stream. The 4 analogue multiplexed input signals from the OPC (A1, A2, CALF and Pw) are filtered by 4 identical LPF's. (One for each channel). This filters can be adapted to various speeds by changing the subsampling factor (i.e. the sample rate of the filter), the cut off frequency scales with the sample frequency. The sample frequency of the filter is equivalent to the OPC timebase frequency, which is the output of the pre-scaler.

9.21 OPC demux.

The OPC demux block demultiplexes the stream supplied by the LPF. This same block also changes the format of the digital data from signed (representation inside the filter) to unsigned (representation in the rest of the OPC). The demultiplexing process introduces one baseclock delay.

9.22 The sequencer.

The OPC sequencer controls the timing of all the hardware actions in the OPC hardware. It generates the OPC timebase and locks it to the ATIP pulse. A programmable pre-scaler generates the OPC timebase.
Dividing the ADC sample clock by 8 derives the input clock of this pre-scaler. (= Identical to the sample rate per channel). The pre-scaler can divide this clock by a number in the range from 1-16. The division factor can be programmed via the OPC ctrl register. The OPC timebase is locked to the selected ATIP source, which can be either an external ATI P sync or an internally generated sync. (Programmable). The OPC timebase clock supplies the sample frequency for the input LPF's, the OPC pre-processor and the EFM detector.
The sequencer controls the timing of all the hardware actions in the OPC hardware. The sequencer is started either by an external ATIP sync or an internally generated sync (programmable).
All data acquisition and alpha0 settings change synchronised to this sync signal (rising edge of the ATIP sync). An exception on this is the switching of the ATIP input itself, which is immediately changed whenever the bit in the OPC ctrl register is changed. When this was latched on the ATIP source itself, it would create a deadlock when there was no ATIPin from CDR-60.

9.23 The Pw monitor

The Pw monitor is used during the "OPC write" and normal write mode. The comparator compares the incoming Pw with two programmable thresholds PW MAX and PW MIN. Both these thresholds can be programmed via the OPC PW register, which contains 4 bits for each threshold.
Internally both 4-bit thresholds PW MAX and PW MIN are extended to 8 bit values. The compare function performs an unsigned compare.
The first threshold is used to detect fingerprints. The second is used to check the correct operation of the laser driver.

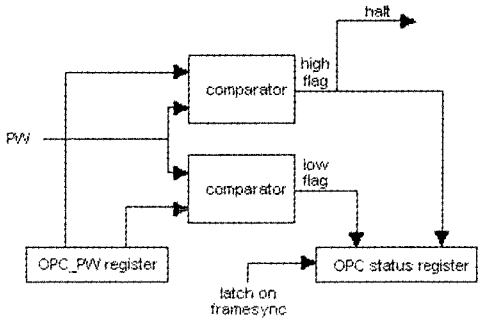


Figure 9-6 OPC PW monitor.

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

FEATURES

- Operates with DVD-ROM,DVD-RAM, DVD+RW, DVD-RW, CD-ROM and CD-RW media
- Operates up to 64x CD-ROM and 8x DVD-ROM
- Support for Dual Light pen DVD systems (DVD/CDRW)
- DVD-RAM (C) playback capability
- DVD-RAM Land-Groove servo polarity switching
- 3 different tracking servo strategies:
  Conventional 3 beam tracking for CD
  Differential Phase Detection (DPD) for DVD-ROM (including option to emulate traditional drop out detection; drop out concealment)
  Advanced Push Pull with dynamic offset compensation for DVD-RAM (recorded and unrecorded areas)
- Radial error signal for fast track counting (FTC)
- 2 different strategies to read header data:
  - Full bandwidth Push Pull signal
  - Left and Right side signal
- Universal photo diode IC interface using internal conversion resistors and offset cancelation
- Flexible adaption to different light pen configurations
- Input buffer amplifiers with low-pass filtering
- RF data amplifier with wide (programmable) bandwidth equivalent to 64xCD / 8x DVD when using equaliser function
- Built-in equalisers cover CAV inner-outer disc range at highest speed.
- Programmable RF gain for DVD-ROM / DVD-RAM / CD-RW / CDROM applications(approx 50dB range)
- Balanced RF-Data signal transfer (single ended still supported)
- Fully automatic laser control including stabilization and an ON/OFF switch, plus a separate supplypin for power efficiency
- Automatic monitor diode polarity selection.
- 3 and 5 V compatible digital interface
- Enhanced signal conditioning in DPD circuit for optimal tracking performance under noisy conditions.

GENERAL DESCRIPTION

The DVDALAS2 is an analogue preprocessor and laser supply circuit for DVD / CD read only players. The device contains data amplifiers, several options for radial tracking and focus control. The preamplifier forms a versatile, programmable interface between dual, voltage output CD/DVD mechanisms to Philips' digital signal processor family for CD and DVD (Gecko, HDR65, Iguano, etc..)

The device contains serval options for radial tracking:
Conventional 3 beam tracking for CD;
Differential Phase Detector (DPD) for DVD;
Push Pull for DVD-RAM with flexible L/R weighing to compensate dynamic offsets e.g. beamlanding offset.
A radial error signal is generated to allow fast track count (FTC) during track jumps.

The dynamic range of this preamp/processor combination can be optimized for the LF servo and RF data paths. The gain in both channels can be programmed separately. This will guarantee an optimal playability for all kind of discs.

Several functions are included to allow playback of DVD-RAM(C) discs:

- The header information can be read via the data output path (RF)
- DC offset compensation techniques provide a fast settling after disc errors.
- Radial servo Polarity switch for land/groove
- two settings for focus offset correction for land and groove

The device can accommodate astigmatic, single foucault and double foucault detectors and can be used with P-type lasers with N- or P-sub monitor diodes. After an initial adjustment, the circuit will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant and stabilized output power is ensured independent of ageing. A separate power supply connection allows the internal power dissipation to be reduced by connecting a low voltage supply.

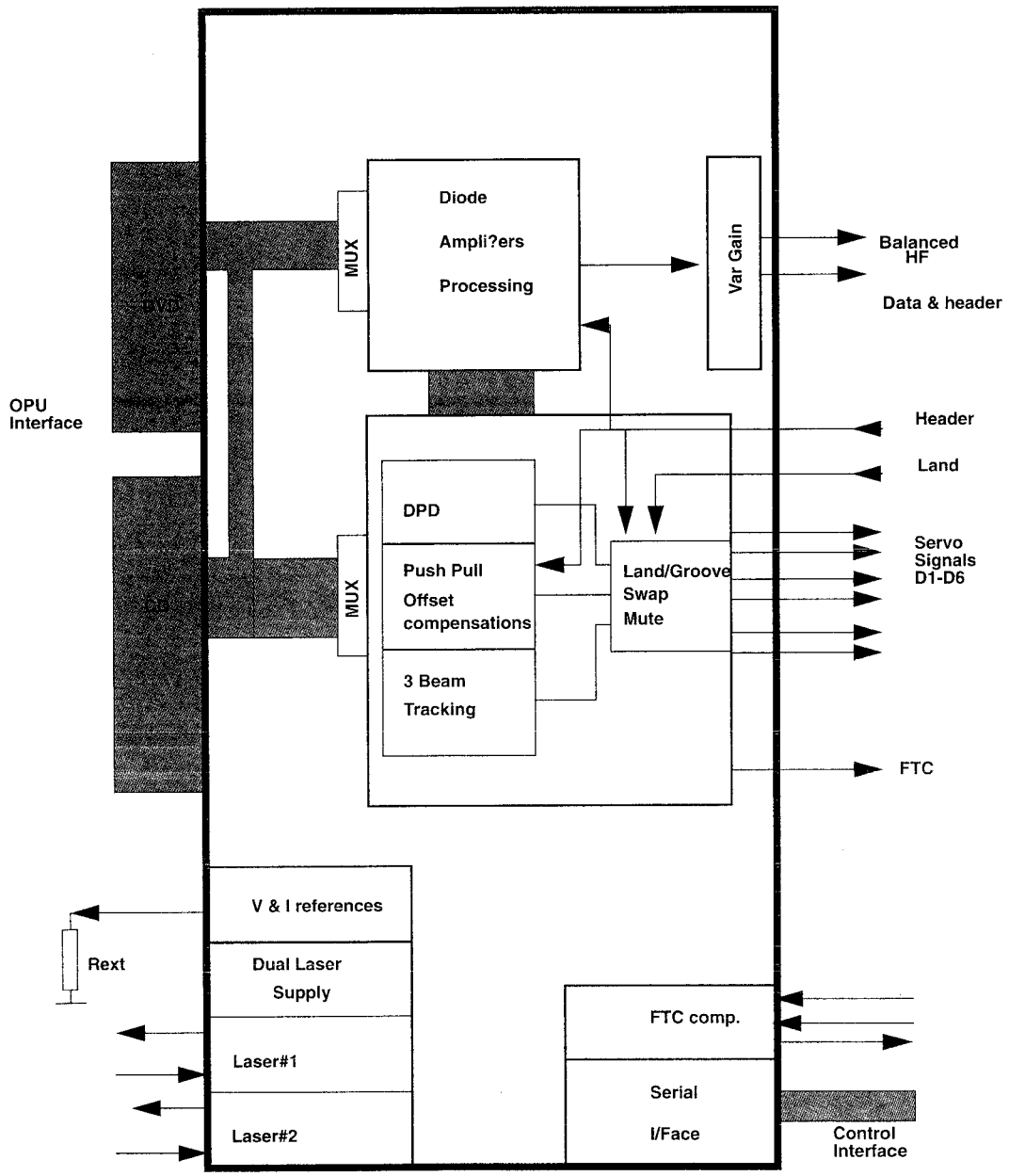
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1023	LQFP64	Plastic low pro?le QFP64; body 10 x 10 x 1.4 mm	SOT314-2

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

DEVICE BLOCK DIAGRAM



DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply — TZA1033

PINNING

Name	Pin	Description
CD-A	1	CD pick up input A
CD-B	2	CD pick up input B
CD-C	3	CD pick up input C
CD-D	4	CD pick up input D
CD-REF	5	CD pick up reference voltage
CD-E	6	CD pick up input E
CD-F	7	CD pick up input F
DVD-A	12	DVD pick up input A
DVD-B	13	DVD pick up input B
DVD-C	14	DVD pick up input C
DVD-D	15	DVD pick up input D
DVD-ref	16	DVD pick up reference voltage
O-A	48	Servo current output for Focus-A
O-B	47	Servo current output for Focus-B
O-C	46	Servo current output for Focus-C
O-D	45	Servo current output for Focus-D
O-central	40	Testpin for offset cancelation
TD2	37	Internally connected
FTC-ref	36	Servo output voltage reference input
S1	42	Servo current output for radial tracking
S2	41	Servo current output for radial tracking
TD1	35	Internally connected
FTC	33	Fast track count voltage output
RFP	55	pos. RF output signal
RFN	56	neg. RF output signal
RF-REF	54	DC Reference signal input RF
LPF-DPD1	38	DPD Low pass bandwidth capacitor, channel pos
LPF-DPD2	39	DPD Low passbandwidth capacitor, channel neg
Land	20	Land/groove toggle input
HEADER	21	Header detector window input
CD-MI	62	CD laser monitor input
DVD-MI	10	DVD laser monitor input
CD-LO	61	CD laser output
DVD-LO	64	DVD laser output
COP	27	Positive inputFTC comparator
COM	28	Inverting inputFTC comparator
COO	29	FTC comparator output

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply — TZA1033

Name	Pin	Description
SIDA	23	Serial host interface data input
SICL	24	Serial host interface clock input
SILD	25	Serial host interface load
VDDA1	8	Analog Supply voltage 1 (RF input)
VDDA2	59	Analog Supply voltage 2 (RF internal)
VDDA3	53	Analog Supply voltage 3 (RF output stage)
VDDA4	44	Analog Supply voltage 4 (Servo)
VDDD5	30	Digital Supply voltage (5V dig core)
VDDD3	22	Digital Supply voltage (3V I/O pads and FTC comp.)
VDDL	63	Supply voltage for laser
VSSA1	9	Analog Ground 1
VSSA2	58	Analog Ground 2
VSSA3	57	Analog Ground 3
VSSA4	43	Analog Ground 4
VSSD	26	Digital ground
Rext	60	Reference current input (Connect 12k1 to VSSA4)
STB	31	Standby input
TM	19	Testmode input
TDO	34	test data out

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

PINNING

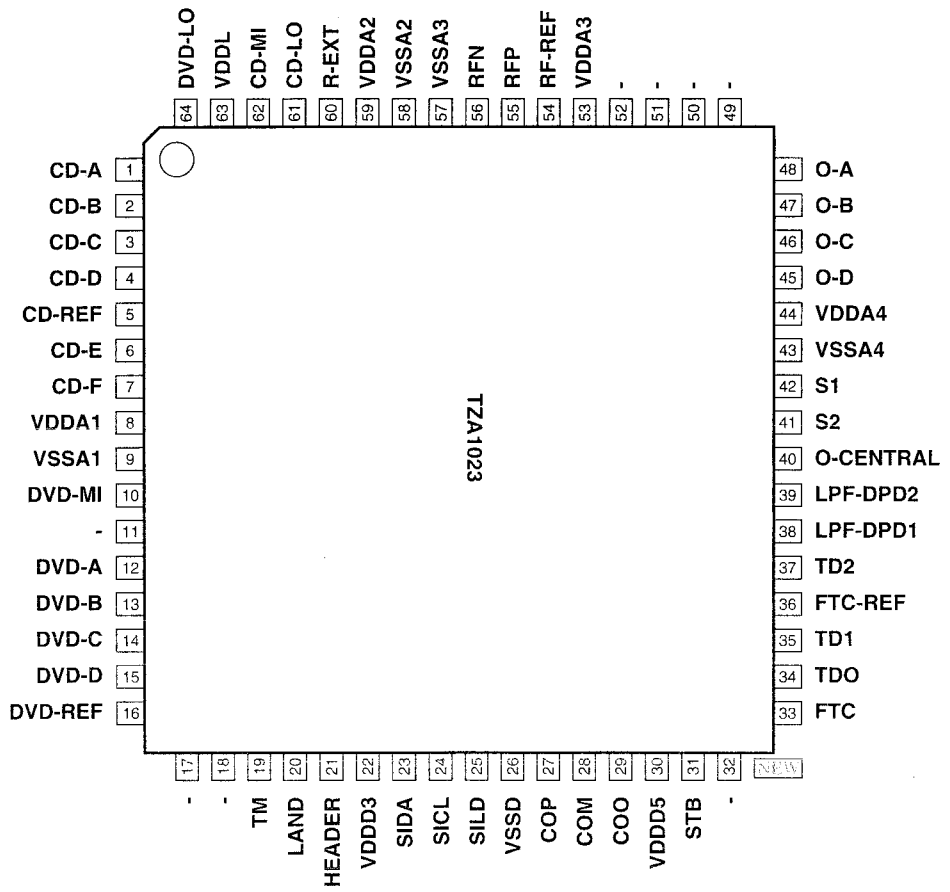


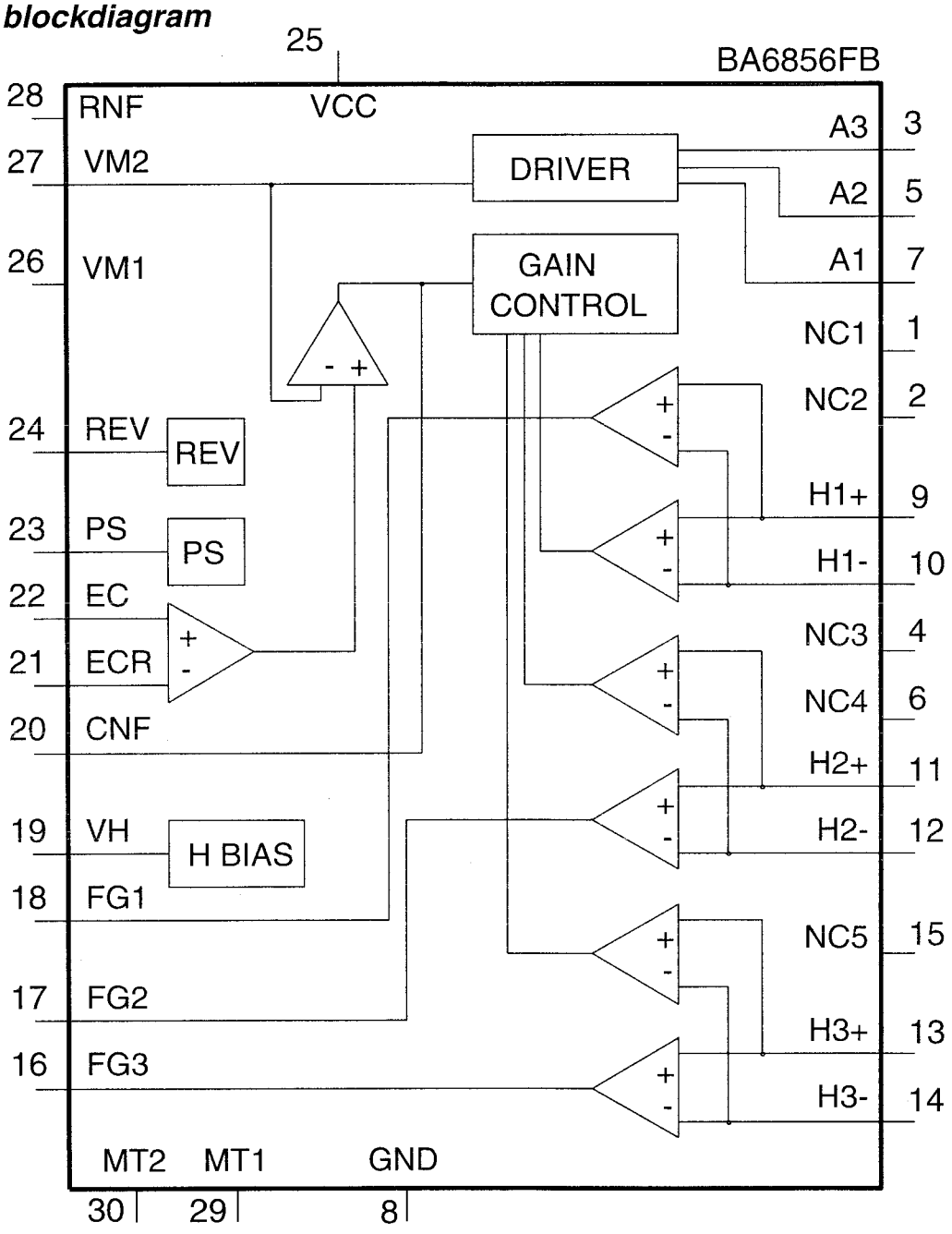
Fig.2 Pin configuration.

BA6856FP: 3 PHASE MOTOR DRIVER FOR DVD PLAYERS

Features

- /3-phase, full-wave pseudo linear driving system
- built-in power save
- built-in therma shut down circuit
- built-in current limit circuit
- built in Hall bias circuit
- built in FG-output (3-phase parallel output)
- with switching function of regular/ reverse rotations

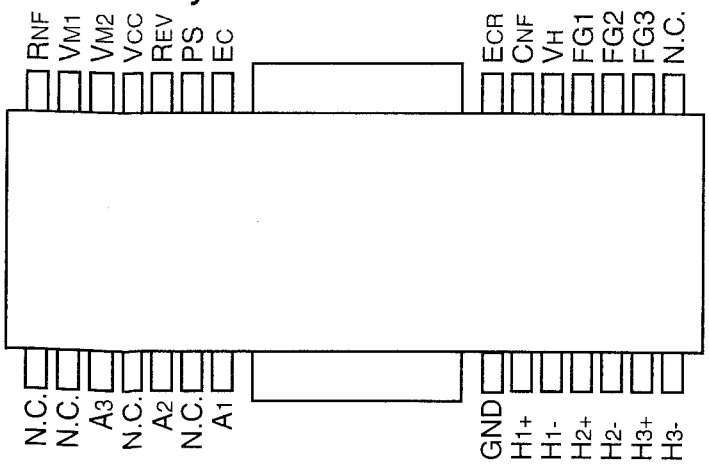
blockdiagram



pin description

PIN No	PIN NAME	DESCRIPTION
1	N.C.	Not connected
2	N.C.	Not connected
3	A_3	Output 3 for motor
4	N.C.	Not connected
5	A_2	Output 2 for motor
6	N.C.	Not connected
7	A_1	Output 1 for motor
8	GND	Ground
9	H_1^+	Hall input Amp1. positive input
10	H_1^-	Hall input Amp1. negative input
11	H_2^+	Hall input Amp2. positive input
12	H_2^-	Hall input Amp2. negative input
13	H_3^+	Hall input Amp3. positive input
14	H_3^-	Hall input Amp3. negative input
15	N.C.	Not connected
16	FG3	FG3 signal output terminal
17	FG2	FG2 signal output terminal
18	FG1	FG1 signal output terminal
19	V_H	Hall Bias
20	C_{NF}	Capacitor connection pin for phase compensation
21	E_{CR}	Torque control standard voltage input terminal
22	E_C	Torque control voltage input terminal
23	PS	POWER SAVE switch
24	R_{FV}	Reverse terminal
25	V_{CC}	Power supply for sinal division
26	V_{M2}	Power supply 2 for driver
27	V_{M1}	Power supply 2 for driver
28	R_{NF}	Power supply for driver division
FIN	FIN	GND

Terminal lay-out



DSP for CD and DVD-ROM systems SAA7335

FEATURES

- Compatibility with CD-I, CD-ROM, MPEG-video DVD-ROM and DVD-video applications
- Designed for very high playback speeds
- Typical CD-ROM operation up to n = 12, DVD-ROM to n = 1.9, maximum rates (tbf)
- Matched filtering, quad-pass error correction (C1-C2-C1-C2), overspeed audio playback function included (up to 3 kbytes buffer)
- Lock-to-disc playback, Constant Angular Velocity (CAV), pseudo-Constant Linear Velocity (CLV) and CLV motor control loops
- Interface to 32 kbytes SRAM for DVD error correction and de-interleave
- Sub-code/ header processing for DVD and CD formats
- Programmable HF equalizer
- In DVD mode it is still compatible with Philips block decoders
- Sub-CPU interface can be parallel or fast I²C-bus
- On-chip clock multiplier.

GENERAL DESCRIPTION

This device is a high-end combined Compact Disc (CD) and Digital Versatile Disc (DVD) compatible decoding device. The device operates with an external 32 kbytes S-RAM memory for de-interleaving operations. The device provides quad-pass error correction for CD-ROM applications (C1-C2-C1-C2) and operates in lock-to-disk, CAV, pseudo CLV and CLV modes.

In DVD modes double-pass C1-C2 error correction is used which is capable of correcting up to 5 C1 frame errors and 16 C2 frame errors.

The SAA7335 contains all the functions required to decode an EFM or EFM+ HF signal directly from the laser pre-amplifier, including analog front-end, PLL data recovery, demodulation and error correction. The spindle motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit.

The SAA7335 has two independent microcontroller interfaces. The first is a serial I²C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to a total of 32 × 8-bit registers for control and status.

This data sheet contains an descriptive overview of the device together with electrical and timing characteristics. For a detailed description of the device refer to the user guide *"SAU/UM96018"*.

Supply of this CD/DVD IC does not convey an implied license under any patent right to use this IC in any CD or DVD application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDD}	digital supply current	–	70	300	mA
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	70	300	mA
f_{xtal}	crystal input frequency	4	25	tbf	MHz
T_{amb}	operating ambient temperature	−20	–	+70	°C
T_{stg}	storage temperature	−55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7335GP	LQFP100	plastic low pro?le quad ?at package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAM

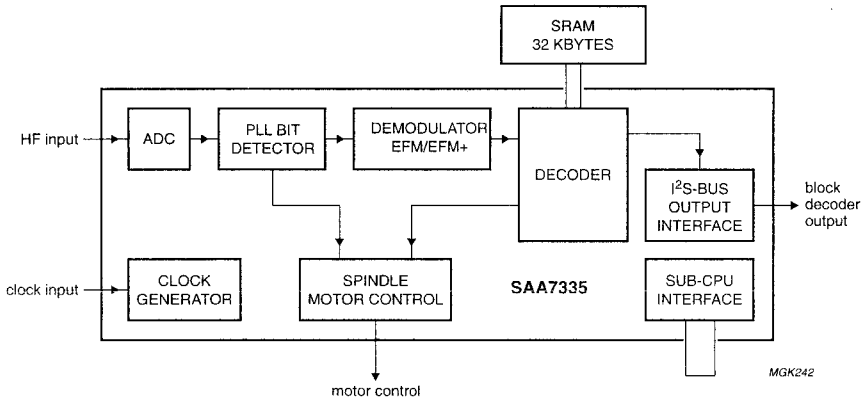


Fig.1 Simplified block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSA1}	1	supply	analog ground 1
I_{ref}	2	I	analog current reference input for ADC
REFLo	3	I	analog low reference input for ADC
REFHi	4	I	analog high reference input for ADC
VREF	5	I	analog negative input
HFIN	6	I	analog positive input
V_{SSA2}	7	supply	analog ground 2
AGCOUT	8	O	analog test pin output
V_{DDA2}	9	supply	analog supply voltage 2
V_{DDD1}	10	supply	digital supply voltage 1
V_{SSD1}	11	supply	digital ground 1
OTD	12	I	off track detect input
MOTO1	13	O	3-state motor control output
n.c.	14	–	not connected, reserved
MOTO2/T3	15	I/O	motor control output/tachometer 3 input
n.c.	16	–	not connected, reserved
T1	17	I	tachometer 1 input
T2	18	I	tachometer 2 input
V_{DDD2}	19	supply	digital supply voltage 2
V_{SSD2}	20	supply	digital ground 2
TEST1	21	I	test input 1
TEST2	22	I	test input 2
POR	23	I	power-on reset input
MUXSWICH	24	I	use clock multiplier input
n.c.	25	–	not connected, reserved
CL1	26	O	divided clock output
BCAIN	27	I	BCA input
SDA	28	I/O	sub-CPU I^2C-bus serial data input/output
SCL	29	I	sub-CPU I^2C-bus serial clock input
INT	30	O	sub-CPU interrupt output (open-drain)
V_{DDD3}	31	supply	digital supply voltage 3
V_{SSD3}	32	supply	digital ground 3
da7	33	I/O	sub-CPU data bus bit 7 input/output (parallel)
da6	34	I/O	sub-CPU data bus bit 6 input/output (parallel)
da5	35	I/O	sub-CPU data bus bit 5 input/output (parallel)
n.c.	36	–	not connected, reserved
da4	37	I/O	sub-CPU data bus bit 4 input/output (parallel)
n.c.	38	–	not connected, reserved
da3	39	I/O	sub-CPU data bus bit 3 input/output (parallel)
da2	40	I/O	sub-CPU data bus bit 2 input/output (parallel)

SYMBOL	PIN	TYPE	DESCRIPTION
da1	41	I/O	sub-CPU data bus bit 1 input/output (parallel)
n.c.	42	–	not connected, reserved
da0	43	I/O	sub-CPU data bus bit 0 input/output (parallel)
V_{DDD4}	44	supply	digital supply voltage 4
V_{SSD4}	45	supply	digital ground 4
$\overline{WRi}$	46	I	sub-CPU write enable input (active LOW)
$\overline{RDi}$	47	I	sub-CPU read enable input (active LOW)
ALE	48	I	sub-CPU address latch enable input
CSi	49	I	sub-CPU chip select input (active HIGH)
STOPCLOCK	50	O	stop clock output
n.c.	51	–	not connected, reserved
V4	52	O	serial subcode output (for CD)
EBUOUT	53	O	digital audio output
SYNC	54	O	I^2S-bus sector sync output
FLAG	55	O	I^2S-bus correction ?ag output
DATA	56	O	I^2S-bus serial data output
BCLK	57	I/O	I^2S-bus bit serial clock input/output
WCLK	58	I/O	I^2S-bus word clock input/output
V_{DDD5}	59	supply	digital supply voltage 5
V_{SSD5}	60	supply	digital ground 5
RAMRW	61	O	RAM read/write control output
n.c.	62	–	not connected, reserved
RAMDA7	63	I/O	RAM data bus bit 7 input/output
RAMDA6	64	I/O	RAM data bus bit 6 input/output
RAMDA5	65	I/O	RAM data bus bit 5 input/output
RAMDA4	66	I/O	RAM data bus bit 4 input/output
RAMDA3	67	I/O	RAM data bus bit 3 input/output
RAMDA2	68	I/O	RAM data bus bit 2 input/output
n.c.	69	–	not connected, reserved
RAMDA1	70	I/O	RAM data bus bit 1 input/output
RAMDA0	71	I/O	RAM data bus bit 0 input/output
V_{DDD6}	72	supply	digital supply voltage 6
V_{SSD6}	73	supply	digital ground 6
RAMAD0	74	O	RAM address bit 0 output
RAMAD1	75	O	RAM address bit 1 output
RAMAD2	76	O	RAM address bit 2 output
RAMAD3	77	O	RAM address bit 3 output
RAMAD4	78	O	RAM address bit 4 output
RAMAD5	79	O	RAM address bit 5 output
RAMAD6	80	O	RAM address bit 6 output
V_{DDD7}	81	supply	digital supply voltage 7

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSD7}	82	supply	digital ground 7
RAMAD7	83	O	RAM address bit 7 output
RAMAD8	84	O	RAM address bit 8 output
RAMAD9	85	O	RAM address bit 9 output
n.c.	86	–	not connected, reserved
RAMAD10	87	O	RAM address bit 10 output
RAMAD11	88	O	RAM address bit 11 output
RAMAD12	89	O	RAM address bit 12 output
RAMAD13	90	O	RAM address bit 13 output
RAMAD14	91	O	RAM address bit 14 output
V_{DDD8}	92	supply	digital supply voltage 8
V_{SSD8}	93	supply	digital ground 8
CRIN	94	I	analog crystal input
CROUT	95	O	analog crystal output
CFLG	96	O	correction statistics output
MEAS1	97	O	front-end telemetry output
V_{DDD9}	98	supply	digital supply voltage 9
V_{SSD9}	99	supply	digital ground 9
V_{DDA1}	100	supply	analog supply voltage 1

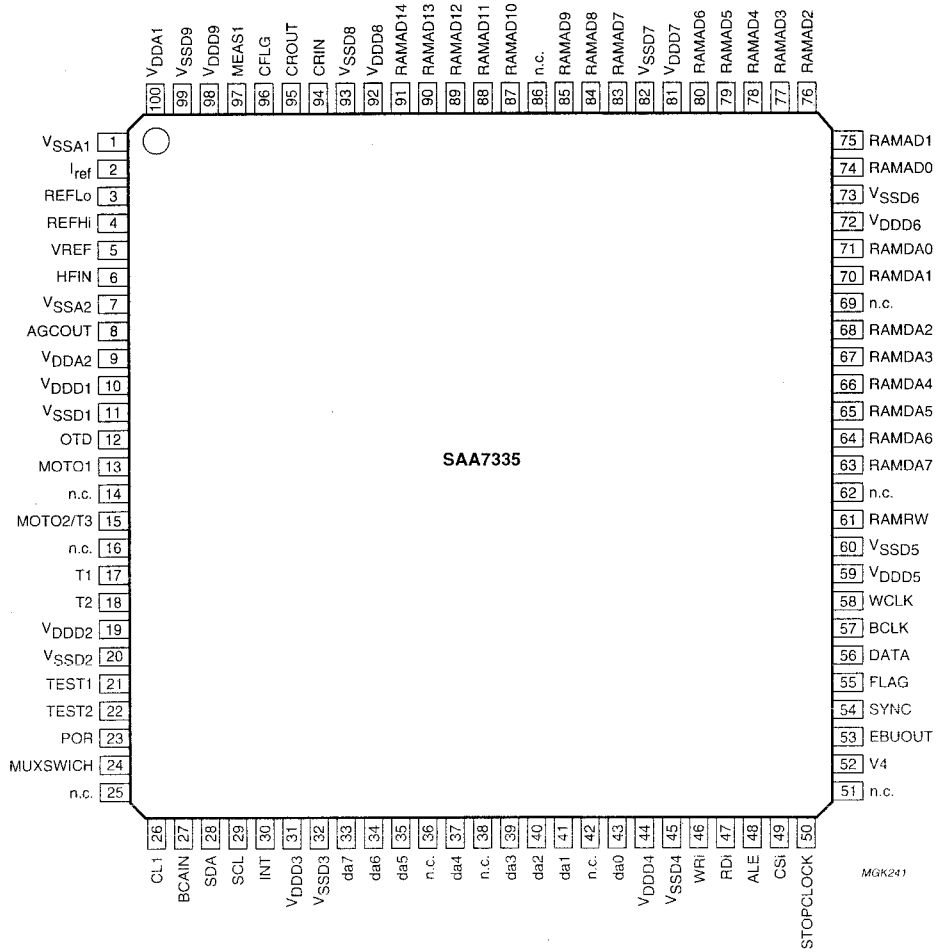


Fig.2 Pin configuration.

DSP for CD and DVD-ROM systems SAA7335

FUNCTIONAL DESCRIPTION

Analog front-end

This block converts the HF input to the digital domain using an 8-bit ADC proceeded by an AGC circuit to obtain the optimum performance from the convertor. This block is clocked by ADCCLK which is set by the external crystal frequency plus a flexible clock multiplier and divider block.

PLL and bit detector

This subsystem recovers the data from the channel stream. The block corrects asymmetry, performs noise filtering and equalisation and finally recovers the bit clock and data from the channel using a digital PLL.

The equalizer and the data slicer are programmable.

Digital logic

All the digital system logic is clocked from the master ADC clock (ADCCLK) described above.

Advanced bit detector

The advanced bit detector offers improved data recovery for multi-layer discs and contains two extra detection circuits to increase the margins in the bit recovery block:

1. Adaptive slicer: adds a second stage slicer with higher bandwidth
2. Run length 2 push-back: all T2 run lengths are pushed back to T3, thereby automatically determining the erroneous edge and shifting the transitions on that edge.

Demodulator

FRAME SYNC PROTECTION CD MODE

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are 588 ±1 EFM clocks apart.
2. The main counter: this is used to partition the EFM signal into 17-bit words. This counter is reset when:
   a) A sync coincidence is generated
   b) A sync is found within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

FRAME SYNC PROTECTION DVD MODE

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are 1488 ±3 EFM+ clocks apart.
2. The main counter: this is used to partition the EFM+ signal into 16-bit words. This counter is reset when:
   a) A sync coincidence is generated
   b) A sync is found within ±10 EFM+ clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

EFM/EFM+ demodulation

The 14-bit EFM (16-bit EFM+) data and subcode words are decoded into 8-bit symbols.

Microcontroller interface

The SAA7335 has two microcontroller interfaces, one serial I²C-bus and one parallel (8051 microcontroller compatible).

The two communication modes may be operated at the same time, the modes are described below:

1. Parallel mode: protocol compatible with 8052 multiplexed bus:
   a) da0 to da7 = address/data bus
   b) ALE = Address Latch Enable, latches the address information on the bus
   c) $\overline{WRi}$ = active LOW write signal for write to SAA7335
   d) $\overline{RDi}$ = active LOW read signal for read from SAA7335
   e) CSi = active HIGH Chip Select signal (this signal gates the $\overline{RDi}$ and $\overline{WRi}$ signals).
2. I²C-bus mode: I²C-bus protocol where SAA7335 behaves as slave device where:
   a) SDA = I²C-bus data
   b) SCL = I²C-bus clock
   c) I²C-bus slave address (write mode) = 3EH
   d) I²C-bus slave address (read mode) = 3FH
   e) Maximum data transfer rate = 400 kbits/s.

MICROCONTROLLER INTERFACE (I²C-BUS MODE)

Bytes are transferred over the interface in single bytes of which there are two types; write data commands and read data commands.

The sequence for a write data command (1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write command address byte
- Write data byte
- Send STOP condition.

The sequence for a read data command (that reads 1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write status address byte
- Send STOP condition
- Send START condition
- Send address 3FH (read)
- Read data byte
- Send STOP condition.

READING AND WRITING DATA TO THE SAA7335

The SAA7335 has 32 × 8-bit configuration and status registers as shown in Table 1. Not all locations are currently defined and some remain reserved for future upgrades. These can be written to or read from via the microcontroller interface using either the serial or parallel control bus.

Am29LV160BT/Am29LV160BB

16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.35 µm process technology**
- **Supports Common Flash Memory Interface (CFI)**
- **High performance**
  - — Full voltage range: access times as fast as 90 ns
  - — Regulated voltage range: access times as fast as 80 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 10 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 write cycle guarantee per sector**
- **Package option**
  - — 48-ball FBGA
  - — 48-ball µBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

GENERAL DESCRIPTION

The Am29LV160B is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, 48-ball µBGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 80, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV160B is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

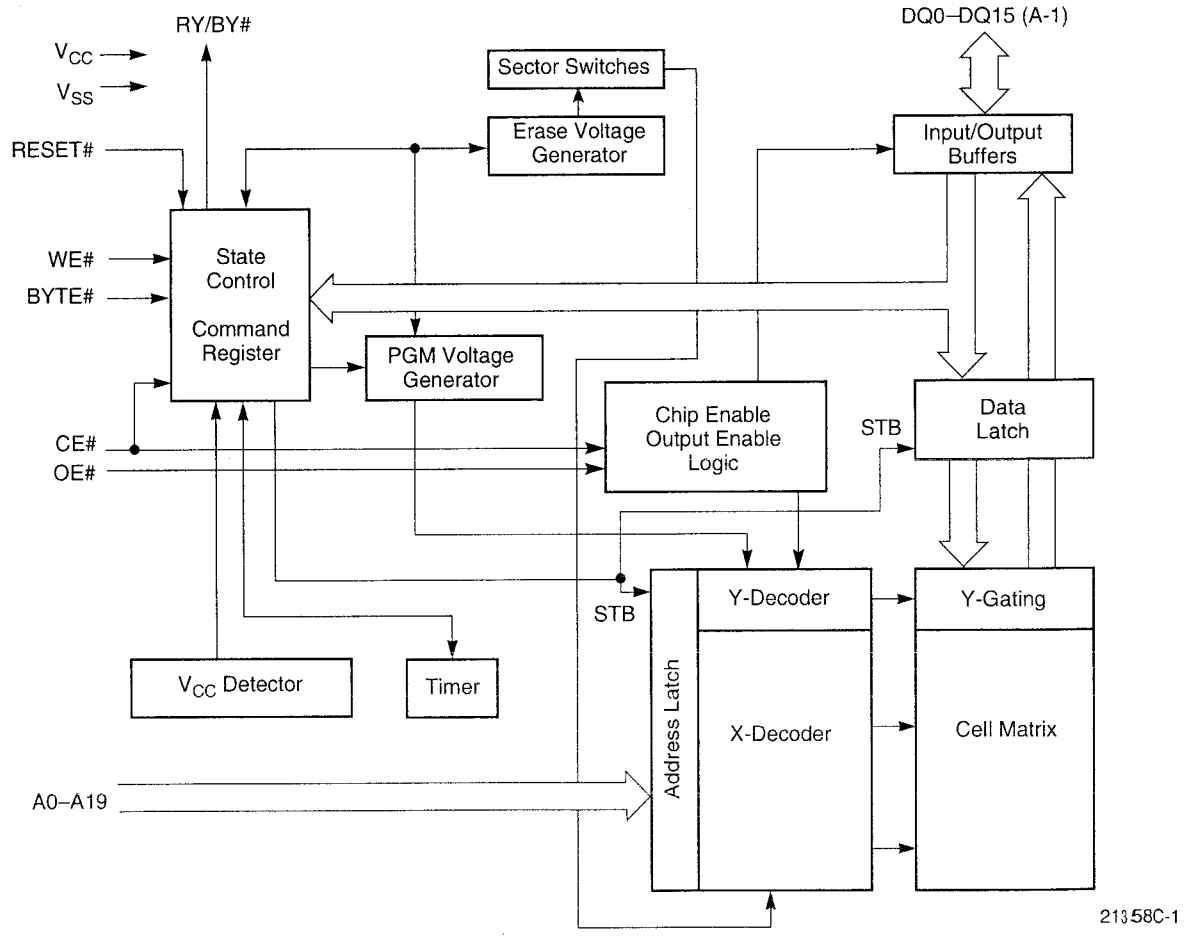
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

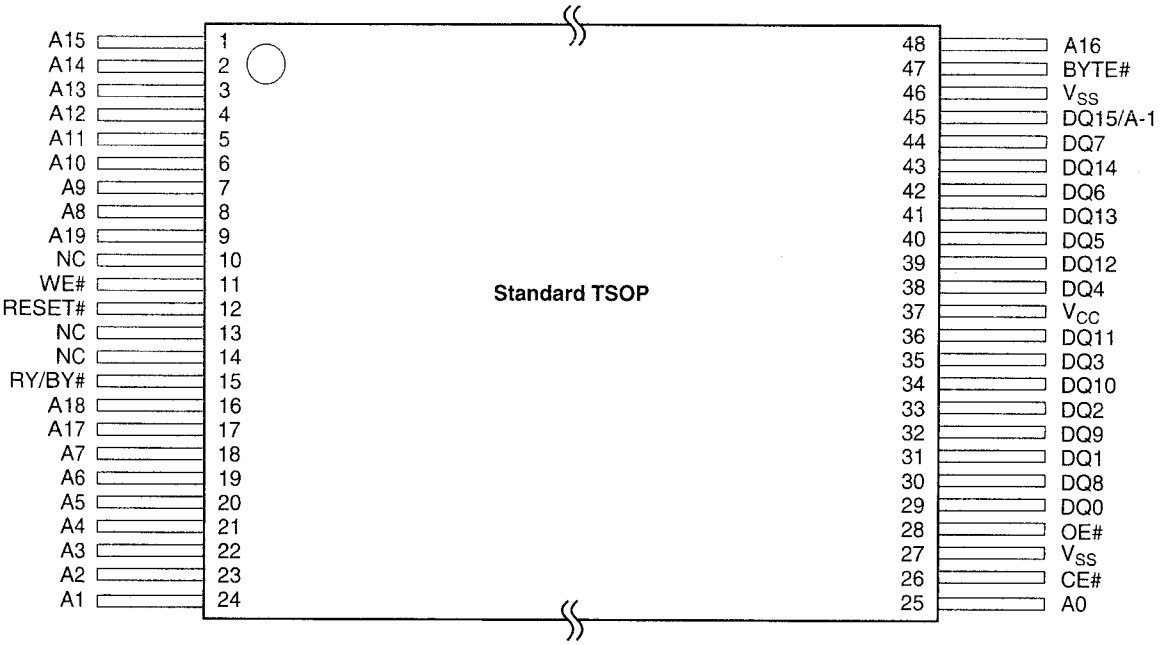
Family Part Number	Am29LV160B		
Ordering Part Number: V_{CC} =3.0–3.6 V	**80R**		
V_{CC} = 2.7–3.6 V		**90**	**120**
Max access time, ns (t_{ACC})	80	90	120
Max CE# access time, ns (t_{CE})	80	90	120
Max OE# access time, ns (t_{OE})	30	35	50

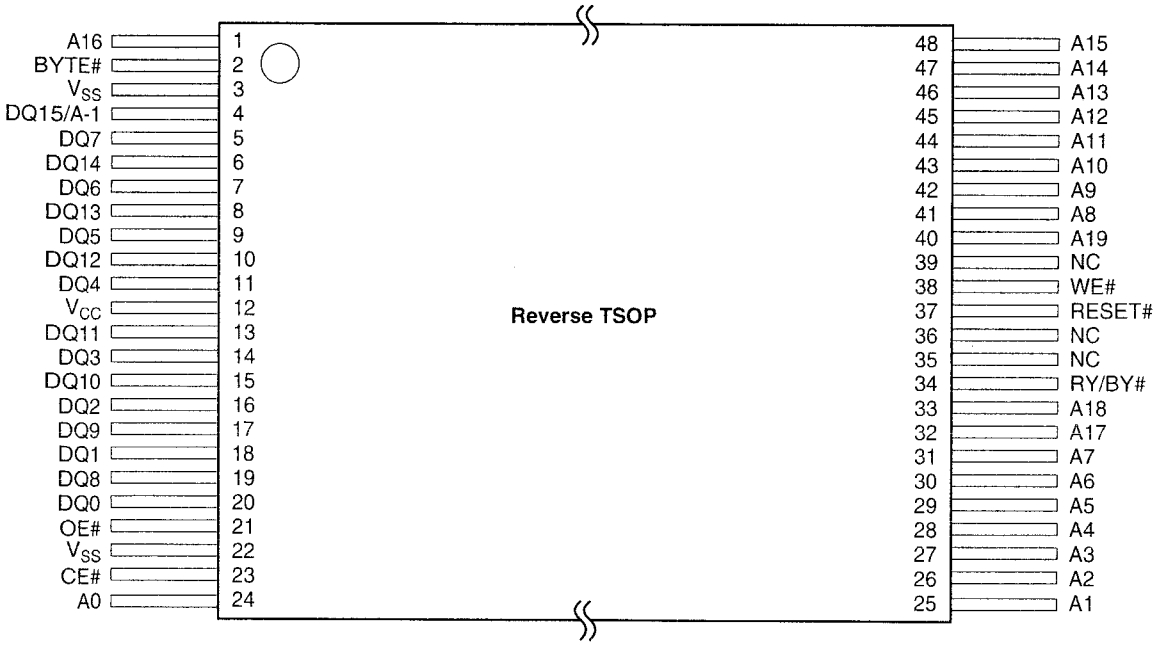
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS





21358C-2

SYNCHRONOUS DRAM

MT48LC1M16A1 S - 512K x 16 x 2 banks

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
  1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT AUTO PRECHARGE
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2 and 3

OPTIONS — MARKING

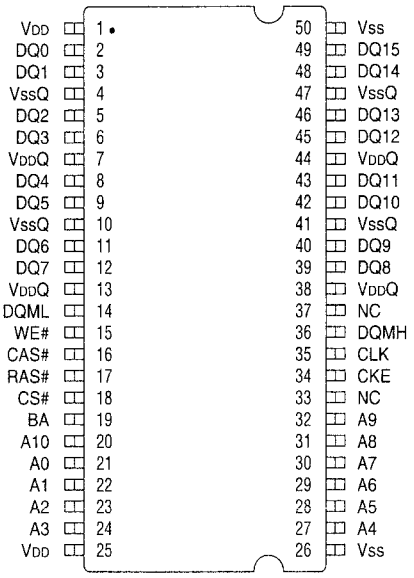
- Configuration
  1 Meg x 16 (512K x 16 x 2 banks) — 1M16A1
- Plastic Package - OCPL*
  50-pin TSOP (400 mil) — TG
- Timing (Cycle Time)
  6ns (166 MHz) — -6
  7ns (143 MHz) — -7
  8ns (125 MHz) — -8A
- Refresh
  2K or 4K with Self Refresh Mode at 64ms — S
- Part Number Example: MT48LC1M16A1TG-7S

KEY TIMING PARAMETERS

SPEED	CLOCK	ACCESS TIME CL = 3**	SETUP	HOLD
-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8A	125 MHz	6ns	2ns	1ns

*Off-center parting line
**CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)
50-Pin TSOP



Note: The # symbol indicates signal is active LOW.

	1 Meg x 16
Configuration	512K x 16 x 2 banks
Refresh Count	2K or 4K
Row Addressing	2K (A0-A10)
Bank Addressing	2 (BA)
Column Addressing	256 (A0-A7)

16Mb (x16) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC1M16A1TG S	1 Meg x 16

GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

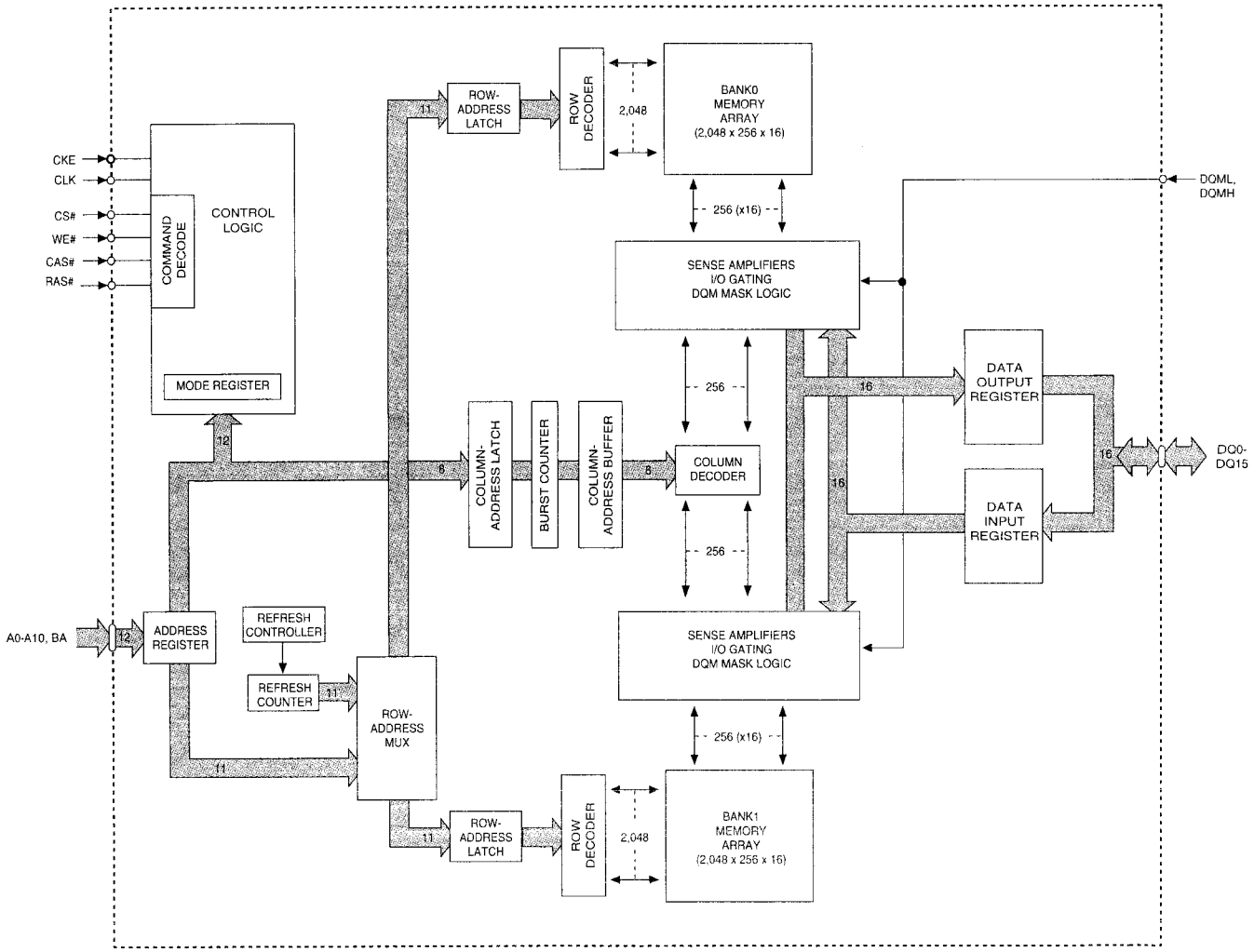
The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

16Mb: x16 SDRAM

FUNCTIONAL BLOCK DIAGRAM
1 Meg x 16 SDRAM



16Mb: x16 SDRAM

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/ Output	Data I/Os: Data bus.
33, 37	NC	–	No Connect: These pins should be left unconnected.
7, 13, 38, 44	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V_{SS}	Supply	Ground.

STi5505 (Rev. Ax)

DVD BACKEND DECODER WITH INTEGRATED HOST PROCESSOR

PRODUCT PREVIEW

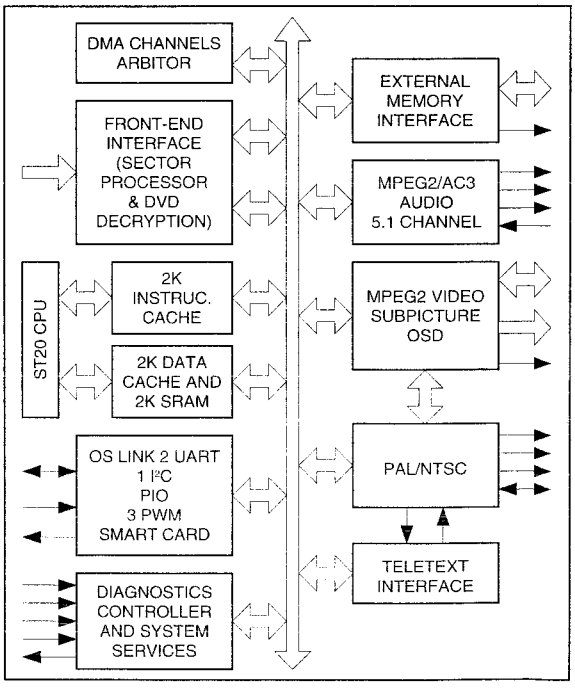
- INTEGRATED 32-BIT RISC HOST CPU
  - 2KBYTES INSTRUCTION CACHE, 2KBYTES DATA CACHE/SRAM
  - 50K DHRYSTONES/SEC (2.1) - 50MHz
- VIDEO DECODER
  - FULLY SUPPORTS MPEG-2 MP@ML
  - MEMORY REDUCTION - PAL IN 12MBITS
- SUBPICTURE DECODER
- HIGH PERFORMANCE ON-SCREEN DISPLAY
- AUDIO DECODER
  - 5.1 CHANNEL DOLBY AC-3® / MULTI CHANNEL MPEG-2 DECODING
  - DOWNMIX TO STEREO OR TO DOLBY PRO-LOGIC COMPATIBLE OUTPUTS FOR MPEG-2 AND AC-3
  - IEC6958 - IEC61937 COMPATIBLE OUTPUT
  - LPCM (DVD) MODE SUPPORTED
  - 6 CHANNELS OUTPUT
- PAL/NTSC ENCODER
  - MACROVISION™ 7.01/6.1 COMPATIBLE
  - TELETEXT, AND CLOSED CAPTION
- HIGH PERFORMANCE SDRAM INTERFACE
- PROGRAMMABLE MEMORY INTERFACE FOR DRAM, ROM, PERIPHERALS ETC.
- FRONT-END CHANNEL IC INTERFACE
  - DVD, VCD AND CD-DA COMPATIBLE
  - DSS - DVB BISTREAMS
  - SERIAL AND PARALLEL INTERFACES
  - HARDWARE SECTOR FILTERING
  - INTEGRATED CSS DECRYPTION AND TRACK BUFFER
- INTEGRATED PERIPHERALS
  - 2 UARTS, 1 I^2C CONTROLLER, 3 PWM OUTPUTS, 3 TIMERS, 3 CAPTURE TIMERS, SMART CARD
  - 34 BITS OF PROGRAMMABLE I/O
  - OS LINK
- PROFESSIONAL TOOLSET SUPPORT
  - ANSI C COMPILER AND LIBRARIES
  - OPERATING SYSTEMS SUPPORT
  - ADVANCED DEBUGGING TOOLS
- 208 PIN PQFP PACKAGE

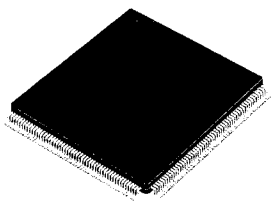
DESCRIPTION

The STi5505 provides a very highly integrated back-end solution for DVD and combo DVD-DVB (Set Top Box) applications. The STi5505 incorporates a host CPU which handles both general application (DVD navigation, CD-DA, VCD, DVB) and drivers of the different embedded periphals (audio/video, subpicture decoders, OSD, PAL/NTSC encoder...).

The STi5505 offers one of the best cost-effective (memory savings, internal peripherals availability) solution to DVD-DVB applications with rapid time to market (Reference design, DVD-DVB Software Toolkit).

Figure 1 : General Block Diagram


DMA CHANNELS ARBITOR
FRONT-END INTERFACE (SECTOR PROCESSOR & DVD DECRYPTION)
ST20 CPU
2K INSTRUC. CACHE
2K DATA CACHE AND 2K SRAM
OS LINK 2 UART 1 I²C PIO 3 PWM SMART CARD
DIAGNOSTICS CONTROLLER AND SYSTEM SERVICES
EXTERNAL MEMORY INTERFACE
MPEG2/AC3 AUDIO 5.1 CHANNEL
MPEG2 VIDEO SUBPICTURE OSD
PAL/NTSC
TELETEXT INTERFACE



PQFP208 (Plastic Quad Flat Pack)
ORDER CODE : STi5505ACV

I - GENERAL DESCRIPTION

The performance offered by the ST20 CPU and its associated hardware (decoders, encoder, peripherals...) allows an integrated and unified DVD or DVD-DVB software solution.

All the following operations are performed inside the STi5505 :

- application management (DVD Navigation, VCD, CD-DA, DVB-Program Guide ...),
- device data retrieval drivers (demultiplex, stream buffer management ...),
- device presentation drivers (video decoder, subpicture decoder, on-screen display, audio decoder, PAL/NTSC encoder ...),
- embedded peripherals drivers (UART, I^2C, Programmable I/O, Smart Card ...).

I.1 - ST20 32-bit CPU

The ST20 micro-core family has been developped by SGS-THOMSON Microelectronics to provide the tools and building blocks to enable the development of highly integrated application-specific 32-bits device at the lowest cost and fastest time to market.

The STi5505 integrates a ST20 C2 core with the following characteristics :

- 50K Dhrystones/s at 50MHz,
- 8/16 bits instructions (32 most common instructions in 8 bits),
- instruction cache 2Kbytes - write back replacement policy,
- internal SRAM 2Kbytes to ensure fast access to critical code, data, interrupt handler ...
- data cache 2 Kbytes - write back replacement policy,

The STi5505's ST20 is provided with advanced debugging tools :

- on-chip real-time emulation,
- debugging with minimal impact on software and performance,
- non intrusive attachment to the host via JTAG (IEEE1149.1),
- no intrusion into the performance of the CPU core,
- no intrusion into user code space by a debug kernel,
- only 40bytes used for breakpoint handler.

I.2 - Video Decoder

The video decoder implemented in the STi5505 uses a patented memory reduction/bandwith reduction scheme to offer the user the best bandwidth/memory size compromise.
The algorithm is lossless and uses "on-the-fly" decoding to reduce the memory requirements to two frame buffers in memory reduction mode.

In this mode, PAL decoding is contained in 12Mbits. When used in bandwith reduction mode, the memory usage is the normal three buffers but the bandwith required by the decoder is significantly reduced compared to a classical implementation.

In summary, the features of the decoder are :

- MPEG-2 Main Profile/Main Level (MP@ML) support,
- MPEG-2 program streams, Packet Elementary streams and MPEG-1 system streams support,
- memory reduction architecture allowing sharing of single 16 Mbits SDRAM between MPEG decoding, micro and transport functions - memory expandable to 32 Mbits of SDRAM,
- letter box (16:9) filter,
- pan-scan, horizontal and vertical image resizing,
- automatic error concealment.

I.3 - Subpicture Decoder

The STi5505 has a hardware DVD compliant subpicture decoder. Subpicture units are copied by DMA into subpicture bit buffer.

The subpicture decoder can decode complete subpicture units without any interaction from the ST20.

The main subpicture decoder features are :

- up to 720x480 or 720x576 subpicture area,
- internal LUTs for Sub Picture, Highlight and PCI (4 bits color and contrast outputs),
- internal color LUT (4 bits from SP, HL, PCI to 24 Y,Cr,Cb bits) for SP color inputs to MPEG, OSD, SP mixer.

I.4 - Audio Decoder

The audio decoder cell is a fully compatible Dolby AC-3™ / MPEG-1/MPEG-2 decoder capable of decoding both 5.1 and 2 channel streams compatible with the DVD standard.

Downmix from 5.1 channels is supported for both Dolby and MPEG-2 streams. The output can be sent directly to external DACs or formatted for transmission in accordance with the IE6958 standard.

The decoder can also handle linear PCM in accordance with the DVD standard. An integrated downsampler is provided for conversion from 96 kHz to 48kHz.

STi5505 (Rev. Ax)

I - GENERAL DESCRIPTION (continued)

The main features of the decoder core are :

- Decodes 5.1 Dolby AC-3 Digital surround,
- Output to 6 channels. Downmix modes : 1, 2, 3 or 4 channels for MPEG and AC-3 streams,
- Karaoke mode for DVD. MPEG-2 capable, AC-3 capable,
- MPEG-1, 2-channel audio decoder layers 1 and 2,
- MPEG-2, 6-channel audio decoder layer 2,
- PCM : transparent. downsampling 96 to 48 kHz,
- Accepts MPEG-2 PES stream format for : MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM,
- IEC6958 Output Interface,
- CD-DA PCM format (subcode output in IEC6958 user data),
- Downmix for Dolby Pro Logic compatible outputs for AC-3 and MPEG-2 (Pro Logic encoder),
- Pro Logic decoder,
- PLL for Internal 44.1 and 48kHz PCM clock generation,
- On chip pink noise generator.

I.5 - High Performance On-Screen Display

The graphics performance of the STi5505 supports the new requirements for intelligent program guides and interactive applications.

The display interface supports up to 256 colors for each OSD region and a transparency feature allows mixing of video with the OSD. Fast access graphics and many other additional features are available and are supported by a graphics library.

Very high system performance is obtained by closely coupling the ST20 RISC processor and cache with the MPEG audio/video core and display memory.

Low latency RISC access and DMA engines allow rapid construction of bit maps.

I.6 - PAL/NTSC Encoder

The STi5505 integrates a PAL/NTSC encoder. It converts the digital MPEG/Sub Picture/OSD stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. Six analog output pins are available on which it is possible to output CVBS, S-VHS (Y/C) and RGB formats.

The encoder handles interlaced and non-interlaced mode.

It can perform Closed Captions, CGMS or Teletext encoding and allows Macrovision 7.01/6.1 copy protection.

The encoder supports both master and slave modes for synchronization.

I.7 - Memory Interfaces

The STi5505 has been designed to minimize system costs by enabling various memory savings. Two kinds of memory interfaces are used on the STi5505 : a programmable External Memory Interface (EMI) and a high performance SDRAM interface.

The External Memory Interface supports several address ranges (memory banks). In each bank, a set of signals are entirely programmable and can be used to map 8/16 bits peripherals such as Front End channel ICs in DVD applications.

The EMI contains a zero glue logic DRAM and a low-cost EPROM interface.

This interface can be programmed to interface very easily peripherals.

The SDRAM memory interface supports gluelessly 125 MHz SDRAMs providing the adequate bandwiths to achieve MPEG decoding and display, OSD drawing and display, and general system use.

Memory savings can be realized on ROM requirements too : the ST20 VL-RISC micro-core has the highest code density of any 32 bit CPU, leading to the lowest cost program ROM.

I.8 - Front-End Interface

The STi5505 's front end interface accepts :

- DVD, VCD and CD-DA sectors,
- DVB-DSS transport stream.

In DVD mode, DVD, VCD and CD-DA information can be input into STi5505 through a serial interface or a generic parallel interface.

In serial mode, data are captured and filtered from I2S and V4 interfaces by an internal sector processor. V4 interface is used to capture VCD and CD-DA subcode information. In parallel mode, sector processor is bypassed.

I - GENERAL DESCRIPTION (continued)

The main features of the DVD interface are :

- DVD, VCD and CD-DA compatible,
- hardware sector filtering,
- subcode error correction for CD-DA,
- integrated CSS decryption,
- integrated track buffer support,
- DMA engine to ST20 memory.

In DVB-DSS mode, DVB-DSS transport stream is input through a serial interface. The STi5505 extracts and descrambles Packet Elementary Streams belonging to one user selected program to be decoded and presented.

The main features of the DVB-DSS interface are :

- descrambling (transport packet and packet elementary streams in DVB mode, transport packet in DSS mode ; up to 32 streams descrambling),
- PID and section filtering,
- clock recovery,
- DMA engine.

In DVB-DSS mode, a high speed digital interface allows to transfer packets between the Set Top Box and external units, either for recording or playback purposes. This interface provides also full support for an external IEEE1394 connection.

I.9 - Integrated Peripherals

Several peripherals generally used in DVD players or DVD-DVB combos have been integrated into the STi5505.

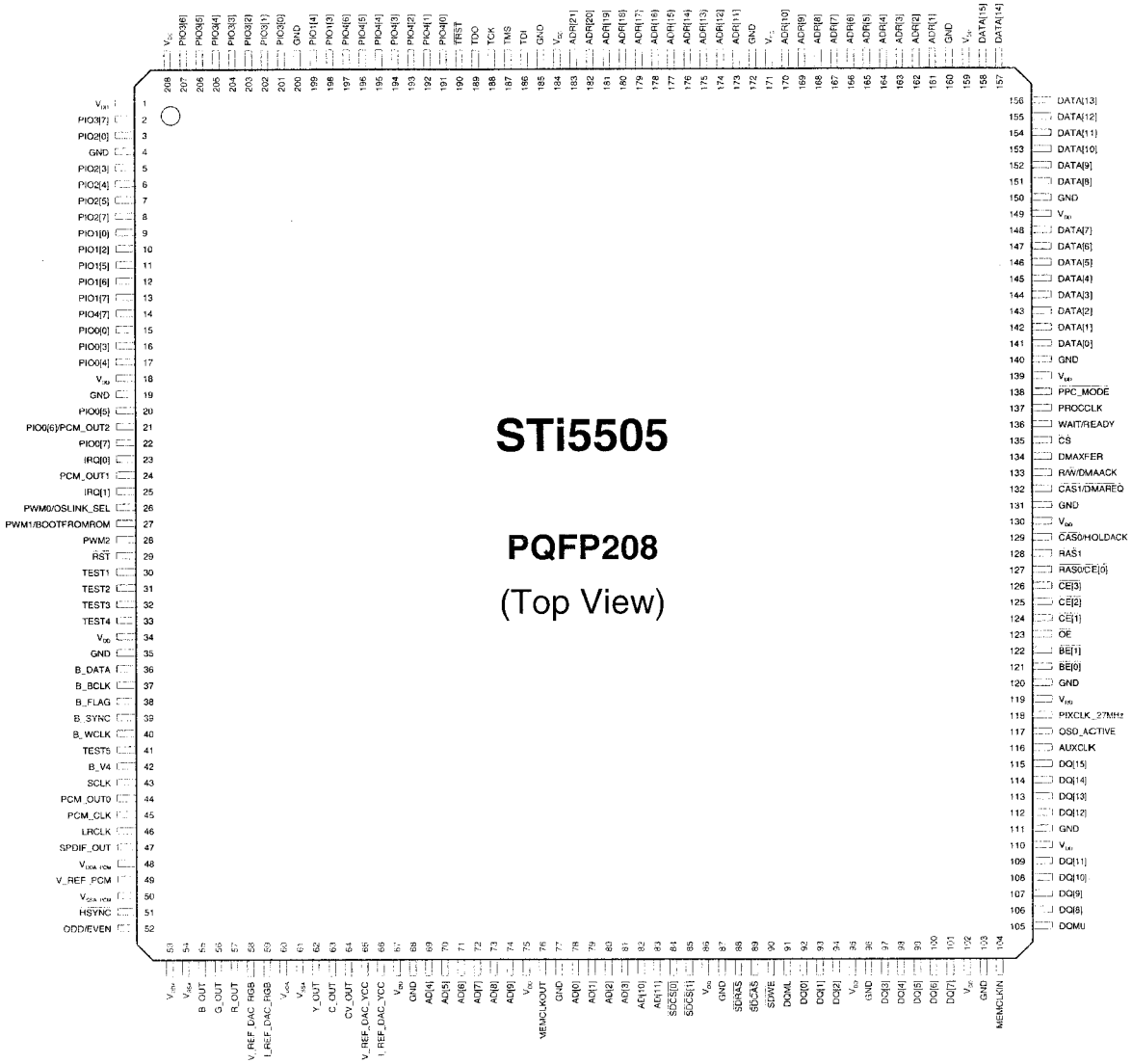
They are :

- two UARTs to interface remote control receivers, DVD front end, modem ...,
- one I^2C controller to interface serial memories, remote control receivers, microcontrollers...,
- 2 SmartCard interfaces (ISO7816-3) for DVB-DSS conditionnal access, pay per view ...,
- PWM/timer module for control of system clock,
- 34 programmable I/O pins,
- OS Link interface,
- JTAG with boundary scan for debug.

STi5505 (Rev. Ax)

II - PIN DESCRIPTION

II.1 - Pin Connections



II - PIN DESCRIPTION (continued)

II.2 - Pin List

Pin	Name	Type	Function
SUPPLIES			
1, 18, 34, 67, 75, 86, 95, 102, 110, 119, 130, 139, 149, 159, 171, 184, 208	V_{DD}		Power Supply
4, 19, 35, 68, 77, 87, 96, 103, 111, 120, 131, 140, 150, 160, 172, 185, 200	GND		Ground
53, 60	V_{DDA}		Analog Power Supply for DENC D/A Converters
54, 61	V_{SSA}		Analog Ground for DENC D/A Converters
48	V_{DDA_PCM}		Analog Power Supply for PLL PCM
49	V_REF_PCM		Analog Reference for PLL PCM
50	V_{SSA_PCM}		Analog Ground for PLL PCM
FRONT-END INTERFACE			
36	B_DATA	I	I^2S Data (DVD) or PARA_DATA[2] (DVD//) or Link Data (DVB/DSS)
40	B_WCLK	I/O	I^2S Word Clock or PARA_DATA[6] (DVD//) or NRSS_CLK (DVB/DSS)
37	B_BCLK	I	I^2S Bit Clock (DVD) or PARA_DATA[3] (DVD//) or Link Bit Clock (DVB/DSS)
38	B_FLAG	I	Error Flag (DVD) or PARA_DATA [4] (DVD//) or Link Sync (DVB/DSS)
39	B_SYNC	I	Sector / Abs Time Sync (DVD) or PARA_DATA[5] (DVD//) or Link Not Valid (DVB/DSS)
42	B_V4	I	Versatile Input Pin (Subcode Input) or PARA_DATA[7] (DVD//) or NRSS_IN (DVB/DSS)
VIDEO OUTPUT INTERFACE			
57	R_OUT	O	Red Output
56	G_OUT	O	Green Output
55	B_OUT	O	Blue Output
63	C_OUT	O	Chroma Output
64	CV_OUT	O	Composite Video Output
62	Y_OUT	O	Luma Output
59	I_REF_DAC_RGB	I	DAC Current Reference
66	I_REF_DAC_YCC	I	DAC Current Reference
58	V_REF_DAC_RGB	I	DAC Voltage Reference
65	V_REF_DAC_YCC	I	DAC Voltage Reference
117	OSD_ACTIVE	I/O	OSD Active
118	PIXCLK_27MHz	I	System Clock Input
51	$\overline{\text{HSYNC}}$	I/O	Horizontal Sync
52	ODD/EVEN	I/O	Vertical Sync
AC-3/MPEG1-2 AUDIO OUTPUT INTERFACE			
43	SCLK	O	Serial Bit Clock
44	PCM_OUT0	O	Audio Serial Output Data 0
24	PCM_OUT1	O	Audio Serial Output Data 1
21	PCM_OUT2	O	Audio Serial Output Data 2
45	PCM_CLK	I/O	PCM Clock In or Out
46	LRCLK	O	Left/Right Clock
47	SPDIF_OUT	O	SPDIF Output

STi5505 (Rev. Ax)

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
EXTERNAL INTERRUPTS			
23, 25	IRQ[0:1]	I	External Interrupts
PROGRAMMABLE I/O AND ALTERNATE FUNCTION (see Device Configuration Chapter)			
15	PIO0 [0]	I/O	General Purpose I/O or PARA_SYNC (DVD//Front End) or Sc1Data (Smart Card 1 Data I/O)
16	PIO0 [3]	I/O	General Purpose I/O or PARA_REQ (DVD//Front End) or Sc1Clk (Smart Card 1 Clock)
17	PIO0 [4]	I/O	General Purpose I/O or PARA_STR (DVD//Front End) or Sc1RST (Smart Card 1 Reset)
20	PIO0 [5]	I/O	General Purpose I/O or PARA_DATA[0] (DVD//Front End) or Sc1Cmd V_{CC} (Smart Card 1 Voltage Enable)
21	PIO0 [6]	I/O	General Purpose IO or Sc1DataDir (Smart Card 1 Dir)
22	PIO0 [7]	I/O	General Purpose I/O or PARA_DATA[1] (DVD//Front End) or Sc1Detect(Smart Card 1 Detect)
9	PIO1 [0]	I/O	General Purpose I/O or I^2C Data
10	PIO1 [2]	I/O	General Purpose I/O or I^2C Clock
198, 199	PIO1 [3:4]	I/O	General Purpose IO
11	PIO1 [5]	I/O	General Purpose IO or ASC1 TXD
12	PIO1 [6]	I/O	General Purpose IO or ASC1 RXD
13	PIO1 [7]	I/O	General Purpose IO or ASC3 TXD
3	PIO2 [0]	I/O	General Purpose I/O or Sc0Data (Smart Card 0 Data I/O)
5	PIO2 [3]	I/O	General Purpose I/O or Sc0Clk (Smart Card 0 Clock)
6	PIO2 [4]	I/O	General Purpose I/O or Sc0RST (Smart Card 0 Reset)
7	PIO2 [5]	I/O	General Purpose I/O or Sc0CmdV_{CC} (Smart Card 0 Voltage Enable)
8	PIO2 [7]	I/O	General Purpose I/O or Sc0Detect (Smart Card 0 Detect)
201	PIO3 [0]	I/O	General Purpose IO or OSLink In
202	PIO3 [1]	I/O	General Purpose IO or OSLink Out
203	PIO3 [2]	I/O	General Purpose IO or CPUReset
204	PIO3 [3]	I/O	General Purpose IO or CPU Analyse
205	PIO3 [4]	I/O	General Purpose IO or ErrorOut
206, 207, 2	PIO3 [5:7]	I/O	General Purpose IO
191-197	PIO4 [0:6]	I/O	General Purpose IO
14	PIO4 [7]	I/O	General Purpose IO or ASC3 RXD
JTAG INTERFACE			
188	TCK	I	Test Clock
186	TDI	I	Test Data Input
189	TDO	O	Test Data Input
187	TMS	I	Test Mode Select
190	$\overline{TRST}$	I	Test Reset
SYSTEM USE			
28	PWM2	O	PWM2 Output
27	PWM1/BOOTFROMROM	O/I	PWM1 Output or Configuration Oslink Pins
26	PWM0/OSLINK_SEL	O/I	PWM0 Output or Boot from ROM during Reset
29	$\overline{RST}$	I	Reset
116	AUXCLK	O	Auxilary Clock for Any Purpose

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
SDRAM INTERFACE			
78-81, 69, 70-74, 82, 83	AD[0:11]	O	SDRAM Address Bus
92-94, 97-101, 106-109, 112-115	DQ[0:15]	I/O	SDRAM Data (Lower Byte)
84, 85	$\overline{\text{SDCS}}$[0:1]	O	SDRAM Chip Selects
89	$\overline{\text{SDCAS}}$	O	SDRAM CAS
88	$\overline{\text{SDRAS}}$	O	SDRAM RAS
90	$\overline{\text{SDWE}}$	O	SDRAM Write Enable
104	MEMCLKIN	I	SDRAM Memory Clock Input
76	MEMCLKOUT	O	SDRAM Memory Clock Output
91	DQML	O	DQ Mask Enable (Lower)
105	DQMU	O	DQ Mask Enable (Upper)
EXTERNAL MEMORY INTERFACE			
161-170, 173-183	ADR[1:21]	I/O	External Memory Address Bus
141-148, 151-158	DATA[0:15]	I/O	External Memory Data Bus
128	$\overline{\text{RAS1}}$/HOLDREQ	O	DRAM RAS or reserved
136	WAIT/READY	I/O	External Wait States or Reserved
133	R/$\overline{\text{W}}$/DMAACK	I/O	DRAM R/$\overline{\text{W}}$ Strobe or Reserved
121, 122	$\overline{\text{BE}}$[0:1]	O	Byte enable
129	$\overline{\text{CAS0}}$/HOLDACK	O/I	DRAM CAS or Reserved
132	$\overline{\text{CAS1}}$/DMAREQ	O	DRAM CAS or Reserved
124-126	$\overline{\text{CE}}$[1:3]	O	Chip Select for Banks 1 - 3
135	$\overline{\text{CS}}$	I	Reserved
137	PROCCLK	I/O	ST20 Clock or Reserved
127	$\overline{\text{RAS0}}$/$\overline{\text{CE0}}$	O	DRAM RAS or Chip Select for Bank 0
134	DMAXFER	I	Reserved
138	$\overline{\text{PPC\_MODE}}$	I	Reserved
123	$\overline{\text{OE}}$	I/O	Output Enable or Reserved
SDAV/P1394 INTERFACE			
30	TEST1	I/O	DATA_RX/STROBE_TX (SDAV Mode) or SDAV_CLK (P1394 Mode)
31	TEST2	I/O	STROBE_RX/DATA_TX (SDAV Mode) or DATA_IN/DATA_OUT (P1394 Mode)
32	TEST3	I/O	Direction (SDAV Mode) or DATA_VALID In/Out (P1394 Mode)
MISCELLANEOUS			
41	TEST5	O	NRSS_OUT (DVB/DSS)

STi5505 (Rev. Ax)

III - FUNCTIONAL DESCRIPTION

III.1 - Functional Modules

Figure 1 shows the subsystem modules that make up the STi5505. These modules are outlined below.

III.1 - CPU

The Central Processing Unit (CPU) on the STi5505 is the ST20-C2 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high speed on-chip SRAM memory, which can store data or programs, and uses the Caches to reduce access time to off chip program and data memory.

The processor can access memory via the general purpose External Memory Interface (EMI) or via the SDRAM EMI which is shared with the MPEG decoder.

III.2 - Memory Subsystem

The STi5505 on-chip SRAM memory system provides 160 Mbytes/s internal data bandwidth, supporting pipelined 2 cycles internal memory access at 25ns cycle times. The STi5505 memory system consists of 2 Kbytes of SRAM, 2Kbytes of instruction cache, a 2Kbytes data cache that can be programmed to be SRAM, and an external memory interface (EMI).

The STi5505 product has 2 Kbytes of on-chip SRAM. The advantage of this is the ability to store time critical code on chip, for instance interrupt routines, software kernels or device drivers, and even frequently used data without these being flushed from the caches.

The instruction and data caches are direct mapped with a write-back system for the data cache and support burst accesses to the external memories for refill and write-back which are effective for increasing performance with page-mode and SDRAM memories.

The STi5505 EMI controls access to the external memory and peripherals while the SDRAM EMI provides access to the SDRAM buffer for the MPEG decoders, ST20 and DMA peripherals.

The STi5505 EMI can access a 16 Mbytes (or greater if DRAM is used) physical address space in each of the four general purpose memory banks, and provides sustained transfer rates of up to 80 Mbytes/s. Peripherals that support an asynchronous data acknowledge are supported as is an external Power PC which can share the bus with the STi5505 and access the SDRAM buffer through the device.

High memory bandwidths up to 200 Mbytes/s can be supported by the SDRAM EMI.

The STi5505 internal memory interconnect provides buffering and arbitration of memory access requests to sustain very high throughput of memory accesses.

III.3 - System Services Module

The STi5505 system services module includes :

- Phase locked loop (PLL) - accepts 27MHz input and generates all the internal high frequency clocks needed for the CPU and the OS-Link.
- test access port - JTAG compatible.
- Diagnostics controller accessed via the JTAG port providing :
- Bootstrapping during development
- Hardware breakpoint and watchpoint
- Real time trace
- External LSA triggering support.

III.4 - Serial Communications

To facilitate the connection of this system the front end device and other peripherals, two UARTs (ASCs) are included in the device. The UARTs provide an asynchronous serial interface.

The UART can be programmed to support a range of baud rates and data formats, for example, data size, stop bits and parity. Two synchronous serial communications (SSC) interfaces are provided on the device. These can be used for a remote control device for example via an I^2C or SPI bus.

III.5 - Interrupt Subsystem

The STi5505 interrupt subsystem supports eight prioritized interrupt levels. Two external interrupt pins are provided. Level assignment logic allows any of the internal or external interrupts to be assigned and, if necessary, share any interrupt level.

III.6 - Front End Interface & DVD Decryption

The front end interface accepts sectors in the case of DVD, MPEG-1 system stream in the case of VCD and PCM data for CD-DA applications on an I2S interface. In the case of VCD and CD-DA disks the subcode information is input via a simple asynchronous serial interface similar to a UART.

The bitstream and subcode stream then pass through a "sector processor" block which handles sector filtering in the case of DVD and sectorizing using the subcode stream for VCD and CD-DA systems.

III - FUNCTIONAL DESCRIPTION (continued)

The block also handles overspeed processing for all systems. The capturing of CD-DA sectors is based on a flywheel tiner to improve robusters by concealing erros in the subcode stream. For DVD the data, having had sector headers removed, then passes through a DVD conformant de-cryption stage and is written into any of the system memories using a programmable DMA engine. When a subcode stream is present it is locally buffered, by subcode block and can be read by the CPU for subsequent processing, if required.

III.7 - PWM and counter module

This unit includes three separate pulse width modulator (PWM) generators using a shared counter, and three timer compare and capture channels sharing a second counter.

The counters can be clocked from a pre-scaled internal clock or from a pre-scaled external clock via the capture clock input and the event on which the timer value is captured is also programmable.

The PWM counters are 8-bit with 8-bit registers to set the output high time. The capture/compare counter and the compare and capture registers are 32-bit.

III.8 - Parallel Programmable IO module

40 bits of parallel I/O are provided. 34 of then are connected to actual PIO pins. Each bit is programmable as an output or an input. The output can be configured as a totem pole or open drain driver. Input compare logic is provided which can generate an interrupt on any change on any input bit.

Many pins of the STi5505 device are multi-function and can either be configured as PIO or connected to an internal peripheral signal.

III.9 - MPEG Video decoder

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps may be superimposed on the display picture through use of the on-screen display function.

III.10 - PAL/NTSC encoder

The digital encoder which is integrated in the STi5505 converts a multiplexed 4:2:2 YUV stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The encoder can also perform closed-caption, CGMS or teletext encoding and allows Macrovision™ 7.01/6.1 copy protection.

III.11 - MPEG-2 Audio / Dolby AC-3 Decoder

The audio decoder is a Dolby AC-3 decoder capable of decoding both 5.1 and 2 channel DVD comformant bitstreams. The decoder also handles MPEG-1 (layers 1 & 2) and MPEG-2 layer 2 (6 channels). Downmix to 2 channels is possible for Dolby and MPEG standards with optional pro-logic encoding.

The decoder directly accepts MPEG-2 PES streams as input. The decoder is capable of supporting IEC6958-IEC61937 formatted outputs for AC-3 and MPEG audio, linear PCM (left & right,16, 18, 20 & 24 bits), zero output (Mute mode) and PCM audio.

ST24E32
ST25E32

32K SERIAL I²C EEPROM with EXTENDED ADDRESSING

NOT FOR NEW DESIGN

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - ± 4.5V to 5.5V for ST24E32 version
  - ± 2.5V to 5.5V for ST25E32 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- ***ST24E32 and ST25E32 are replaced by the M24C32***

PSDIP8 (B)
0.25mm Frame

SO8 (M)
200mil Width

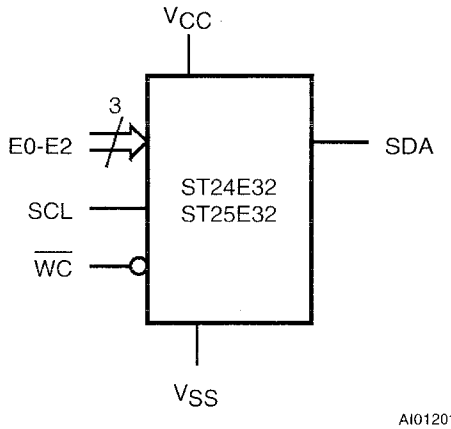
DESCRIPTION

The ST24/25E32 are 32K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST25E32 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



ST24E32, ST25E32

Figure 2A. DIP Pin Connections

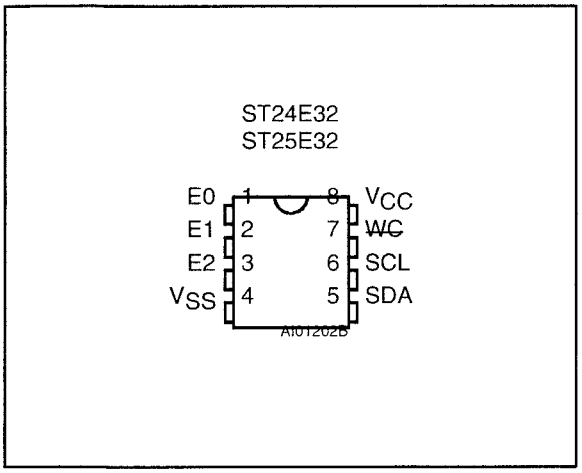


Figure 2B. SO Pin Connections

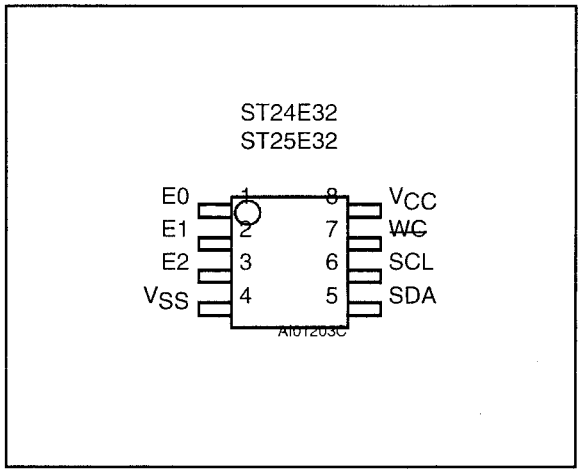


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			±40 to 125	°C
T_{STG}	Storage Temperature			±65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			±0.6 to 6.5	V
V_{CC}	Supply Voltage			±0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E32carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E32 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

10. Spare parts list

VAL6011

Various

0001	3139 197 60090	GENEVA LP LOADER ASSY
0002	9305 022 60101	VAM6001/01
0003	3139 194 00710	SUSPENSION
0004	3139 194 00710	SUSPENSION
0005	3139 194 00620	SUSPENSION
0006	3139 194 00620	SUSPENSION
0007	3139 197 60060	CLAMPER ASSEMBLY

Loader

Various

0004	4822 358 10266	
0009	3139 198 80010	
0010	4822 532 13097	TULE
0011	3139 194 00270	
0012	3139 197 50060	

Monoboard

Various

1104	2422 025 15963	CON BM H 24P F 0.50 FFC SMD R
1106	2422 025 16158	CON BM H 8P F 1.00 FFC 0.3 R
1205	2422 540 98428	RES CER SM 8M467 CSTCC8.46MHz R
1300	2422 540 98426	RES CER SM 6MHz CSTCC6.00MHz R
1301	4822 267 51454	CONN. 11P FEMALE
1603	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1604	2422 025 16388	CON BM V 16P F 1.00 FFC 0.3 R

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2100	4822 126 14305	100nF 10% 16V 0603
2101	4822 126 14305	100nF 10% 16V 0603
2103	4822 124 80151	47µF 16V
2104	4822 126 13193	4.7nF 10% 63V
2105	4822 122 33761	22pF 5% 50V
2107	4822 126 13956	68pF 5% 63V CASE 0603
2108	4822 126 14315	390pF 5% 50V 0603
2109	2020 552 95697	
2110	2222 861 15222	50V 2N2 PM5
2111	4822 126 14305	100nF 10% 16V 0603
2112	5322 126 11578	1nF 10% 50V 0603
2113	4822 126 14305	100nF 10% 16V 0603
2114	4822 122 31765	100pF 2% 63V
2115	4822 126 14305	100nF 10% 16V 0603
2116	4822 126 14305	100nF 10% 16V 0603
2117	4822 126 14305	100nF 10% 16V 0603
2120	4822 126 14305	100nF 10% 16V 0603
2121	4822 126 13879	220nF 20% 16V
2123	4822 126 14305	100nF 10% 16V 0603
2124	4822 126 14305	100nF 10% 16V 0603
2125	4822 126 14305	100nF 10% 16V 0603
2126	4822 126 14305	100nF 10% 16V 0603
2127	4822 126 14305	100nF 10% 16V 0603
2128	4822 126 14508	180pF 5% 50V 0603
2129	4822 126 14508	180pF 5% 50V 0603
2130	4822 122 33761	22pF 5% 50V
2131	4822 126 14494	22nF 10% 25V 0603
2136	4822 126 14305	100nF 10% 16V 0603
2137	4822 126 14305	100nF 10% 16V 0603
2138	4822 126 14305	100nF 10% 16V 0603
2139	4822 126 14305	100nF 10% 16V 0603
2140	4822 126 14241	0603 50V 330P COL R
2141	4822 122 33761	22pF 5% 50V
2142	5322 126 11583	10nF 10% 50V 0603
2143	4822 126 13883	220pF 5% 50V
2144	4822 126 13883	220pF 5% 50V
2145	4822 126 13883	220pF 5% 50V
2203	4822 126 14305	100nF 10% 16V 0603
2204	4822 126 14305	100nF 10% 16V 0603
2205	4822 126 14305	100nF 10% 16V 0603
2206	4822 126 14549	33nF 16V O6O3
2207	5322 126 11578	1nF 10% 50V 0603
2208	4822 126 14305	100nF 10% 16V 0603
2209	4822 126 14305	100nF 10% 16V 0603
2210	5322 126 11578	1nF 10% 50V 0603
2212	4822 126 14305	100nF 10% 16V 0603
2213	4822 126 14305	100nF 10% 16V 0603
2215	4822 124 23237	22µF 6.3V
2216	5322 126 11578	1nF 10% 50V 0603
2226	4822 126 14305	100nF 10% 16V 0603
2227	4822 126 14305	100nF 10% 16V 0603
2228	4822 126 14305	100nF 10% 16V 0603
2300	4822 126 14305	100nF 10% 16V 0603
2301	4822 126 14305	100nF 10% 16V 0603
2302	4822 126 14305	100nF 10% 16V 0603
2303	4822 124 80349	47µF 20% 6.3V
2306	4822 124 23002	10µF 16V
2309	4822 126 14305	100nF 10% 16V 0603
2310	4822 126 14305	100nF 10% 16V 0603
2314	4822 126 14305	100nF 10% 16V 0603
2315	4822 126 14305	100nF 10% 16V 0603
2318	5322 122 33861	120pF 10% 50V
2319	4822 126 11669	27pF
2401	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 126 14305	100nF 10% 16V 0603
2404	4822 126 14305	100nF 10% 16V 0603
2405	4822 126 14305	100nF 10% 16V 0603
2406	4822 126 14305	100nF 10% 16V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2408	4822 126 14305	100nF 10% 16V 0603
2409	4822 126 14305	100nF 10% 16V 0603
2410	4822 126 14305	100nF 10% 16V 0603
2411	4822 126 14305	100nF 10% 16V 0603
2412	4822 126 14305	100nF 10% 16V 0603
2413	4822 126 14305	100nF 10% 16V 0603
2418	4822 124 12095	100µF 20% 16V
2419	4822 124 80349	47µF 20% 6.3V
2420	4822 124 80349	47µF 20% 6.3V
2500	4822 126 14305	100nF 10% 16V 0603
2502	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2503	4822 126 14305	100nF 10% 16V 0603
2504	4822 122 31765	100pF 2% 63V
2505	4822 126 14494	22nF 10% 25V 0603
2506	4822 124 23002	10µF 16V
2507	4822 126 14305	100nF 10% 16V 0603
2508	5322 126 11579	3.3nF 10% 63V
2509	4822 126 14241	0603 50V 330P COL R
2510	4822 126 14305	100nF 10% 16V 0603
2511	4822 126 14305	100nF 10% 16V 0603
2512	4822 126 14305	100nF 10% 16V 0603
2513	4822 126 14305	100nF 10% 16V 0603
2514	4822 126 14305	100nF 10% 16V 0603
2515	4822 126 14305	100nF 10% 16V 0603
2516	4822 126 14305	100nF 10% 16V 0603
2517	4822 126 14305	100nF 10% 16V 0603
2518	4822 126 14305	100nF 10% 16V 0603
2519	4822 126 14305	100nF 10% 16V 0603
2520	4822 126 14305	100nF 10% 16V 0603
2521	4822 126 14305	100nF 10% 16V 0603
2522	4822 126 14305	100nF 10% 16V 0603
2523	4822 126 14305	100nF 10% 16V 0603
2524	4822 126 14305	100nF 10% 16V 0603
2525	4822 126 14305	100nF 10% 16V 0603
2526	4822 126 14305	100nF 10% 16V 0603
2527	4822 126 14305	100nF 10% 16V 0603
2528	4822 126 14305	100nF 10% 16V 0603
2529	4822 126 14305	100nF 10% 16V 0603
2530	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2531	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2532	4822 122 33777	47pF 5% 63V
2533	4822 122 33777	47pF 5% 63V
2534	5322 126 11578	1nF 10% 50V 0603
2535	5322 126 11578	1nF 10% 50V 0603
2600	4822 126 14494	22nF 10% 25V 0603
2601	4822 126 14247	0603 50V 1N5 COL R
2602	4822 126 14247	0603 50V 1N5 COL R
2603	4822 126 14305	100nF 10% 16V 0603
2604	4822 124 12095	100µF 20% 16V
2605	4822 126 14494	22nF 10% 25V 0603
2606	4822 124 12095	100µF 20% 16V
2607	4822 124 12095	100µF 20% 16V
2608	4822 124 23002	10µF 16V
2609	4822 124 80151	47µF 16V
2610	4822 126 14305	100nF 10% 16V 0603
2611	4822 124 12095	100µF 20% 16V
2614	4822 122 33777	47pF 5% 63V
2615	4822 122 33777	47pF 5% 63V
2616	4822 122 33777	47pF 5% 63V
2617	4822 122 33777	47pF 5% 63V
2618	4822 126 14305	100nF 10% 16V 0603
2619	4822 126 14305	100nF 10% 16V 0603
2620	4822 122 33777	47pF 5% 63V
2621	4822 122 33777	47pF 5% 63V
2622	4822 122 33777	47pF 5% 63V
2623	4822 122 33777	47pF 5% 63V
2624	4822 122 33777	47pF 5% 63V
2625	4822 122 33777	47pF 5% 63V
2626	4822 122 33777	47pF 5% 63V
2627	4822 122 33777	47pF 5% 63V
2632	4822 124 12095	100µF 20% 16V
2633	4822 124 12095	100µF 20% 16V
2634	4822 126 14305	100nF 10% 16V 0603
2635	4822 126 14305	100nF 10% 16V 0603
2636	4822 126 14305	100nF 10% 16V 0603
2637	4822 126 14305	100nF 10% 16V 0603
2638	4822 126 14305	100nF 10% 16V 0603
2639	4822 126 14305	100nF 10% 16V 0603

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3100	4822 117 11152	4Ω7 5%
3102	5322 117 13034	1k5 1% 0.063W 0603 RC22H
3103	5322 117 13034	1k5 1% 0.063W 0603 RC22H
3104	5322 117 13062	390Ω 1% 0.063W 0603 RC22H
3105	4822 051 30103	10k 5% 0.062W
3106	4822 051 30479	47Ω 5% 0.062W
3107	4822 051 20228	2Ω2 5% 0.1W
3108	4822 051 20228	2Ω2 5% 0.1W
3110	4822 051 30479	47Ω 5% 0.062W
3111	5322 117 13058	150Ω 1% 0.063W 0603 RC22H
3112	5322 117 13021	47Ω 1% 0.063W 0603 RC22H
3114	4822 051 20228	2Ω2 5% 0.1W
3115	4822 051 20228	2Ω2 5% 0.1W
3116	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3117	4822 051 30181	180Ω 5% 0.062W
3118	4822 051 30681	680Ω 5% 0.062W
3119	5322 117 13062	390Ω 1% 0.063W 0603 RC22H
3120	4822 051 30102	1k 5% 0.062W
3121	4822 051 30273	27k 5% 0.062W
3122	4822 051 30471	470Ω 5% 0.062W
3123	4822 051 30103	10k 5% 0.062W
3124	4822 051 30471	470Ω 5% 0.062W
3125	4822 051 30103	10k 5% 0.062W
3126	4822 051 30103	10k 5% 0.062W
3127	4822 051 30223	22k 5% 0.062W
3128	2322 704 69109	
3129	4822 051 30392	3k9 5% 0.063W 0603
3130	4822 051 20228	2Ω2 5% 0.1W
3131	4822 051 20228	2Ω2 5% 0.1W
3132	4822 051 20228	2Ω2 5% 0.1W
3133	4822 051 20228	2Ω2 5% 0.1W
3134	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3135	4822 117 13613	2Ω2 5% 0603
3137	4822 117 13613	2Ω2 5% 0603
3138	5322 117 13053	6k8 1% 0.063W 0603 RC22H
3139	4822 117 12917	1Ω 5% 0.062W CASE0603
3140	4822 051 30479	47Ω 5% 0.062W
3141	4822 117 11152	4Ω7 5%
3142	5322 117 13028	12k 1% 0.063W 0603 RC22H
3143	5322 117 13043	220Ω 1% 0.063W 0603 RC22H
3144	2322 704 69109	
3146	4822 051 30103	10k 5% 0.062W
3147	4822 051 30103	10k 5% 0.062W
3148	5322 117 13022	22k 1% 0.063W 0603 RC22H
3153	4822 117 12139	22Ω 5% 0.062W
3155	4822 051 30103	10k 5% 0.062W
3157	4822 051 30103	10k 5% 0.062W
3158	5322 117 13017	100Ω 1% 0.063W 0603 RC22H
3160	4822 051 30101	100Ω 5% 0.062W
3161	4822 117 13613	2Ω2 5% 0603
3162	4822 051 30101	100Ω 5% 0.062W
3163	4822 051 30273	27k 5% 0.062W
3164	4822 117 13613	2Ω2 5% 0603

3165	5322 117 13063	120Ω 1% 0.063W 0603 RC22H
3166	4822 051 30393	39k 5% 0.062W
3167	4822 051 30101	100Ω 5% 0.062W
3168	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3169	4822 051 30101	100Ω 5% 0.062W
3170	4822 051 30101	100Ω 5% 0.062W
3171	4822 051 30101	100Ω 5% 0.062W
3172	4822 117 13632	100k 1% 0603 0.62W
3173	4822 117 13632	100k 1% 0603 0.62W
3174	4822 117 11152	4Ω7 5%
3175	4822 117 13613	2Ω2 5% 0603
3176	4822 051 30153	15k 5% 0.062W
3178	4822 117 11151	1Ω 5%
3179	4822 051 30221	220Ω 5% 0.062W
3180	4822 117 13632	100k 1% 0603 0.62W
3181	4822 051 30561	560Ω 5% 0.062W
3182	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3183	5322 117 13017	100Ω 1% 0.063W 0603 RC22H
3184	2322 704 61204	
3185	4822 117 11151	1Ω 5%
3187	4822 051 30273	27k 5% 0.062W
3189	4822 051 30008	0Ω jumper
3190	4822 051 30008	0Ω jumper
3191	4822 051 30008	0Ω jumper
3192	4822 051 30008	0Ω jumper
3193	4822 051 30008	0Ω jumper
3194	4822 051 30008	0Ω jumper
3195	4822 051 30008	0Ω jumper
3197	4822 051 30008	0Ω jumper
3198	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3199	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3200	4822 051 30103	10k 5% 0.062W
3201	4822 117 11151	1Ω 5%
3202	4822 117 11151	1Ω 5%
3203	4822 051 30105	1M 5% 0.062W
3204	4822 051 30331	330Ω 5% 0.062W
3205	4822 051 30103	10k 5% 0.062W
3206	4822 051 30103	10k 5% 0.062W
3208	4822 051 30272	2k7 5% 0.062W
3209	4822 051 30472	4k7 5% 0.062W
3210	4822 051 30392	3k9 5% 0.063W 0603
3211	4822 051 30472	4k7 5% 0.062W
3212	4822 117 11152	4Ω7 5%
3213	4822 117 11152	4Ω7 5%
3214	4822 051 30392	3k9 5% 0.063W 0603
3215	4822 051 30103	10k 5% 0.062W
3219	4822 051 30103	10k 5% 0.062W
3220	4822 051 30103	10k 5% 0.062W
3221	4822 051 30103	10k 5% 0.062W
3224	4822 051 30151	150Ω 5% 0.062W
3225	2322 704 62004	
3226	4822 051 30103	10k 5% 0.062W
3227	4822 051 30472	4k7 5% 0.062W
3229	4822 051 30123	12k 5% 0.062W
3230	4822 051 30103	10k 5% 0.062W
3231	4822 051 30103	10k 5% 0.062W
3232	4822 117 13613	2Ω2 5% 0603
3234	4822 117 12902	8k2 1% 0.063W 0603
3235	4822 117 13632	100k 1% 0603 0.62W
3236	4822 051 30472	4k7 5% 0.062W
3237	4822 051 30103	10k 5% 0.062W
3238	4822 051 30103	10k 5% 0.062W
3239	4822 051 30103	10k 5% 0.062W
3240	4822 051 30103	10k 5% 0.062W
3242	4822 051 30008	0Ω jumper
3243	4822 051 30008	0Ω jumper
3246	4822 051 30008	0Ω jumper
3247	4822 051 30008	0Ω jumper
3249	4822 051 30008	0Ω jumper
3250	4822 051 30008	0Ω jumper
3251	4822 051 30008	0Ω jumper
3252	4822 051 30008	0Ω jumper
3253	4822 051 30008	0Ω jumper
3254	4822 051 30008	0Ω jumper
3255	4822 051 30008	0Ω jumper
3256	4822 051 30008	0Ω jumper
3257	4822 051 30008	0Ω jumper
3258	4822 051 30008	0Ω jumper
3259	4822 117 11151	1Ω 5%
3260	4822 117 11151	1Ω 5%
3300	4822 117 11152	4Ω7 5%
3301	4822 051 30105	1M 5% 0.062W
3302	4822 051 30221	220Ω 5% 0.062W
3304	4822 051 30272	2k7 5% 0.062W
3305	4822 051 30272	2k7 5% 0.062W
3309	4822 051 30103	10k 5% 0.062W
3310	4822 051 30223	22k 5% 0.062W
3311	4822 051 30223	22k 5% 0.062W
3312	4822 051 30472	4k7 5% 0.062W
3313	4822 051 30472	4k7 5% 0.062W
3316	4822 051 20108	1Ω 5% 0.1W
3317	4822 051 20108	1Ω 5% 0.1W
3318	4822 051 30472	4k7 5% 0.062W
3319	4822 051 30479	47Ω 5% 0.062W
3320	4822 051 30472	4k7 5% 0.062W
3321	4822 051 30682	6k8 5% 0.062W
3322	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3323	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3324	4822 117 13632	100k 1% 0603 0.62W
3325	4822 051 30682	6k8 5% 0.062W
3326	4822 051 30479	47Ω 5% 0.062W
3327	4822 051 30682	6k8 5% 0.062W
3328	4822 051 30223	22k 5% 0.062W
3329	4822 051 30223	22k 5% 0.062W
3330	4822 051 30223	22k 5% 0.062W
3331	4822 051 30332	3k3 5% 0.062W
3332	4822 051 30332	3k3 5% 0.062W
3333	4822 051 30101	100Ω 5% 0.062W
3334	4822 051 30101	100Ω 5% 0.062W
3335	4822 051 30101	100Ω 5% 0.062W
3336	4822 051 30101	100Ω 5% 0.062W
3337	4822 051 30101	100Ω 5% 0.062W
3338	4822 051 30101	100Ω 5% 0.062W
3339	4822 051 30008	0Ω jumper
3340	4822 051 30008	0Ω jumper
3403	4822 051 30103	10k 5% 0.062W
3404	4822 051 30103	10k 5% 0.062W
3405	4822 051 30103	10k 5% 0.062W
3412	4822 051 30008	0Ω jumper
3414	4822 051 30008	0Ω jumper
3416	4822 051 30008	0Ω jumper
3500	4822 051 30332	3k3 5% 0.062W
3501	4822 051 30332	3k3 5% 0.062W
3502	4822 051 30223	22k 5% 0.062W
3503	4822 051 30103	10k 5% 0.062W
3504	4822 051 30103	10k 5% 0.062W
3505	4822 051 30103	10k 5% 0.062W
3506	4822 051 30103	10k 5% 0.062W
3507	4822 051 30472	4k7 5% 0.062W
3508	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3509	4822 051 30103	10k 5% 0.062W
3511	4822 051 30332	3k3 5% 0.062W
3512	4822 051 30332	3k3 5% 0.062W
3513	4822 051 30103	10k 5% 0.062W
3514	4822 051 30103	10k 5% 0.062W
3515	4822 051 30103	10k 5% 0.062W
3516	4822 051 30103	10k 5% 0.062W
3517	4822 051 30332	3k3 5% 0.062W
3519	4822 051 30103	10k 5% 0.062W
3520	4822 051 30103	10k 5% 0.062W
3521	4822 051 30103	10k 5% 0.062W
3522	4822 051 30103	10k 5% 0.062W
3523	4822 051 30332	3k3 5% 0.062W
3524	4822 051 30101	100Ω 5% 0.062W
3525	4822 051 30103	10k 5% 0.062W
3526	4822 051 30103	10k 5% 0.062W
3534	4822 051 30103	10k 5% 0.062W
3535	4822 051 30153	15k 5% 0.062W
3536	4822 051 30101	100Ω 5% 0.062W
3537	4822 051 30331	330Ω 5% 0.062W
3538	4822 051 30681	680Ω 5% 0.062W
3541	4822 051 30479	47Ω 5% 0.062W
3542	4822 051 30479	47Ω 5% 0.062W
3545	4822 051 30221	220Ω 5% 0.062W
3546	4822 051 30101	100Ω 5% 0.062W
3548	4822 051 30008	0Ω jumper
3549	4822 051 30008	0Ω jumper
3550	4822 051 30101	100Ω 5% 0.062W
3551	4822 051 30101	100Ω 5% 0.062W
3552	4822 051 30008	0Ω jumper
3554	4822 051 30008	0Ω jumper
3564	4822 051 30008	0Ω jumper
3566	4822 051 30008	0Ω jumper
3570	4822 051 30101	100Ω 5% 0.062W
3571	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3572	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3605	4822 051 30008	0Ω jumper
3606	4822 117 12925	47k 1% 0.063W 0603
3607	4822 117 13632	100k 1% 0603 0.62W
3608	4822 117 13632	100k 1% 0603 0.62W
3609	4822 117 13632	100k 1% 0603 0.62W
3610	4822 051 30103	10k 5% 0.062W
3611	4822 051 30103	10k 5% 0.062W
3612	4822 051 30103	10k 5% 0.062W
3613	4822 051 30103	10k 5% 0.062W
3614	4822 051 30103	10k 5% 0.062W
3615	4822 051 30103	10k 5% 0.062W
3616	4822 051 30103	10k 5% 0.062W
3618	4822 051 30223	22k 5% 0.062W
3619	4822 051 30223	22k 5% 0.062W
3620	4822 051 30101	100Ω 5% 0.062W
3621	4822 051 30101	100Ω 5% 0.062W
3622	4822 051 30101	100Ω 5% 0.062W
3623	4822 051 30101	100Ω 5% 0.062W
3624	4822 051 30101	100Ω 5% 0.062W
3625	4822 051 30101	100Ω 5% 0.062W
3626	4822 051 30102	1k 5% 0.062W
3627	4822 051 30471	470Ω 5% 0.062W
3628	4822 051 30471	470Ω 5% 0.062W
3629	4822 051 30472	4k7 5% 0.062W
3630	4822 051 30221	220Ω 5% 0.062W
3631	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3632	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3633	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3635	4822 051 30682	6k8 5% 0.062W
3636	4822 051 30682	6k8 5% 0.062W
3637	4822 051 30332	3k3 5% 0.062W
3642	4822 051 30103	10k 5% 0.062W
3647	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3648	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3651	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3654	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3655	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3656	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3657	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3658	4822 051 30102	1k 5% 0.062W
3659	4822 051 30102	1k 5% 0.062W
3660	4822 051 30102	1k 5% 0.062W
3661	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3662	4822 051 30102	1k 5% 0.062W
3663	4822 051 30102	1k 5% 0.062W
3664	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3665	4822 117 12139	22Ω 5% 0.062W
3667	4822 051 30331	330Ω 5% 0.062W
3669	4822 051 30008	0Ω jumper
3670	4822 051 30008	0Ω jumper
3671	4822 051 30223	22k 5% 0.062W
3672	4822 051 30479	47Ω 5% 0.062W
3673	4822 051 30101	100Ω 5% 0.062W
3677	4822 051 30008	0Ω jumper
3678	4822 051 30008	0Ω jumper
3679	4822 051 30008	0Ω jumper
3681	4822 051 30008	0Ω jumper
3683	4822 051 30008	0Ω jumper
3685	4822 051 30008	0Ω jumper
3686	4822 051 30223	22k 5% 0.062W
3687	4822 051 30223	22k 5% 0.062W
3688	4822 051 30472	4k7 5% 0.062W
3689	4822 051 30223	22k 5% 0.062W

5200	4822 157 11717	BLM31P500SPT
5300	4822 157 11717	BLM31P500SPT
5301	4822 157 11717	BLM31P500SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5501	4822 157 70299	2.2µH (NL322522T-2R2J)
5502	4822 157 70299	2.2µH (NL322522T-2R2J)
5503	4822 157 71206	BLM21A601SPT
5504	4822 157 71206	BLM21A601SPT
5600	4822 157 71206	BLM21A601SPT
5601	4822 157 11499	BLM11P600SPT
5602	4822 157 10547	15µH 5%
5603	4822 157 71206	BLM21A601SPT
5604	4822 157 10547	15µH 5%
5605	4822 157 10547	15µH 5%
5606	4822 157 10547	15µH 5%
5607	4822 157 10547	15µH 5%
5608	4822 157 10547	15µH 5%
5609	4822 157 11717	BLM31P500SPT
5610	4822 157 11717	BLM31P500SPT

6200	4822 130 11397	BAS316
6301	9322 128 69685	S1D

6302	9322 128 69685	S1D
6303	9322 128 69685	S1D
6600	4822 130 11528	1PS76SB10

7100	5322 130 42718	BFS20
7101	5322 130 42718	BFS20
7102	9352 637 37518	
7103	4822 209 17229	BA5938FM
7104	4822 209 30095	LM833D
7105	4822 209 32073	MC34072D
7106	5322 130 42718	BFS20
7109	4822 209 15083	AN78M09
7110	5322 130 60803	BST72A
7111	5322 130 60159	BC846B
7112	5322 130 60159	BC846B
7113	5322 130 60159	BC846B
7114	5322 130 60159	BC846B
7115	4822 130 60373	BC856B
7116	5322 130 60159	BC846B
7201	9351 869 80118	
7202	3104 123 95660	
7203	4822 130 60373	BC856B
7207	9352 636 60557	SAA7399HL/M2A
7304	4822 209 16877	BA6856FP
7310	4822 209 15899	CY7C199-15C
7311	9352 622 13557	SAA7335HL
7312	4822 130 60373	BC856B
7315	5322 130 60159	BC846B
7401	9322 132 01668	AM29LV160B
7404	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7405	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7501	5322 130 60159	BC846B
7503	9322 151 16671	IC SM STI5505AVC (ST00) Y
7504	4822 242 10838	27MHZ 120P FX0-31FT
7505	8204 056 05580	IC SM M24C32-WMN6TNKSA
7600	5322 209 71568	PC74HCT14T
7604	5322 130 60159	BC846B
7605	4822 209 17398	LD1117DT33
7607	5322 130 60159	BC846B
7608	4822 130 60373	BC856B
7609	4822 130 60373	BC856B
7610	5322 130 60159	BC846B
7611	9352 456 80115	
7612	5322 130 60159	BC846B
7613	5322 130 60159	BC846B
7614	5322 130 60159	BC846B
7615	5322 130 60159	BC846B
7616	4822 209 16062	MK2742-03S
7617	5322 130 60159	BC846B
7618	5322 130 60159	BC846B
7620	4822 130 60373	BC856B
7621	4822 130 42804	BC817-25